Packaging of Microwave Integrated Circuits in LTCC Technology

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La vie, c'est comme une bicyclette,
il faut avancer pour ne pas perdre l'équilibre
— Albert Einstein —

A mes chers parents, mes soeurs et mon frère pour leur patience et leur soutien . . .
A mon épouse pour ses encouragements et son amour . . .
A tous ceux qui ont été à mes côtés pour gravir le plus haut échelon. . .

Abstract

This thesis concerns the introduction and development in our laboratory of a multilayer ceramic technology, called LTCC, for RF and microwave packaging. LTCC stands for Low Temperature Co-fired Ceramics. As can be understood from its name, the low temperature means that the LTCC circuit is fired below $1000°C$ *that allows the use of high conductivity materials such as gold and silver. The thesis work starts after the bibliographic study of RF packaging technology, with the choice of LTCC substrate and conductor materials necessary to implement LTCC technology in our laboratory. Then, the LTCC manufacturing process is put in place and validated in order to produce operational LTCC circuits. This process includes the cut of LTCC layers, via hole and cavity creation, via fill for vertical interconnecting, screen printing for horizontal patterns, stacking, lamination and finally the firing to obtain a 3D circuit. Most encountered technological problems are resolved and the fabrication steps are validated. LTCC* DESIGN RULES *that contain all dimensional values required for future RF packaging designers at the laboratory is elaborated. Next, after the successful establishment of LTCC technology, it is qualified up to* 40 GHz *using simple RF structures such as transmission lines and planar resonators. Then, a multilayer LTCC package for an MMIC oscillator functioning in the frequency band between* 10.6 *and* 12.6 GHz *is proposed, fabricated and finally measured.*

Key words: LTCC technology, manufacturing process, RF packaging, Design Rules, MMIC integration, RF measurement.

Résumé court

L'objectif de cette thèse est d'introduire et développer dans notre laboratoire une technologie multi-couches sur céramique, appelée LTCC, pour la mise en boîtier de circuits RF et hyper-fréquences. LTCC désigne une technologie "céramique co-cuite à basse température" (Low Temperature Co-fired Ceramic). Comme son nom l'indique, "basse température" signifie que le circuit LTCC est cuit en dessous de $1000°C$*, ce qui permet l'utilisation de matériaux à haute conductivité tels que l'or et l'argent. Après l'étude de l'état de l'art des différentes technologies de mise en boîtier RF, le travail de thèse a consisté à choisir les matériaux nécessaires pour la mise en place de la technologie LTCC au laboratoire. Ensuite, le procédé de fabrication a été validé par une série de tests afin de produire des circuits LTCC fonctionnels. Ce procédé inclut la découpe des couches LTCC, la création des trous et des cavités, le remplissage des trous pour assurer la liaison verticale entre les couches, la sérigraphie des motifs horizontaux, l'empilement et le pressage pour obtenir un circuit en 3D et finalement la cuisson pour obtenir un circuit monobloc. Les différents problèmes technologiques rencontrés ont été résolus et les étapes de fabrication sont validées. Les règles de conception de circuits en technologie LTCC, qui regroupent toutes les dimensions nécessaires pour de futures conceptions de boîtiers RF au laboratoire, sont mises en place. Après la mise en place de la technologie LTCC, celle-ci a été validée dans le domaine RF jusqu'à* 40 GHz *en utilisant des structures RF simples telles que des lignes de transmission et des résonateurs planaires. Enfin, un boîtier multicouche intégrant un oscillateur MMIC en puce fonctionnant dans une bande de fréquence de* 2 GHz *entre* 10.6 *and* 12.6 GHz *a été conçu, fabriqué et mesuré.*

Mots clés : technologie LTCC, procédé de fabrication, mise en boîtiers RF, règles de conception, intégration MMIC, mesure RF.

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KHODOR RIDA BREST, SEPTEMBER 2013

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List of Acronyms

3D	Three Dimensional
ADS	Advanced Design System
BGA	Ball Grid Array
CAD	Computer Aided Design
CBCPW	Conductor Backed Coplanar Waveguide
CNC	Computer Numerical Control
CPW	Coplanar Waveguide
CSP	Chip Scale Package
DC	Direct Current
DIP	Dual In line Package
DRC	Design Rule Check
EM	Electro-Magnetic
FEM	Finite Element Method
FGCPW	Finite Ground Coplanar Waveguide
FMCW	Frequency Modulated Continuous Wave
GPS	Global Positioning Systems
HDI	High Density Integration
HFSS	High Frequency Structure Simulator
HTCC	High Temperature Co-fired Ceramic
IC	Integrated Circuit
IPA	Iso Propyl Alcohol
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTCC	Low Temperature Co-fired Ceramic
MCM	Multi Chip Module
MIM	Metal Insulation Metal
MEMS	Micro Electro Mechanical Systems
MoM	Momentum Method

MMIC	Monolithic Microwave Integrated circuit
Nd-YAG	Neodymium-doped Yttrium Aluminum Garnet
PCB/PWB	Printed Circuit/Wiring Board
QFP	Quad Flat Package
RF	Radio Frequency
SCP	Single Chip Package
SiP	System in Package
SOIC	Small Outline Integrated Circuit
SOLT	Short Open Load Thru
SMT	Surface Mount Technique
TAB	Tape Automated Bonding
TE	Transverse Electric
TEM	Transverse Electro-Magnetic
TM	Transverse Magnetic
TRL	Thru Reflect Line
UV	Ultra-Violet
VCO	Wireless Local Area Network
WLAN	Wireless Local Area Network

List of Symbols

α	Attenuation
Z_0	Characteristic impedance
σ	Conductor conductivity
α_c	Conductor loss
ϵ	Complex permittivity
α_d	Dielectric loss
ε_{eff}	Effective dielectric permittivity
c	Free-space velocity
f	Frequency
Hz	Hertz
$\tan\delta$	Loss tangent
Ω	Ohm
μ	Permeability
ε_r	Relative permittivity
ρ	Resistivity
R_s	Sheet resistance
δ_s	Skin depth
rgh	Surface roughness
TCE	Thermal Coefficient of Expansion
Q	Quality factor
λ	Wavelength

Al_2O_3	Alumina
Al	Aluminum
AlN	Aluminum Nitride
BeO	Beryllia or Beryllium Oxide
B_2O_3	Boron trioxide
CaO	Calcium oxide
CO_2	Carbon dioxide
Cu	Copper
$GaAs$	Gallium Arsenide
Au	Gold
$Au-Pd$	Gold-Palladium
$Au-Pt$	Gold-Platinum
PbO	Lead Monoxide
MgO	Magnesium Oxide
Mo	Molybdenum
Si	Silicon
SiO_2	Silicon Dioxide or Silica
Ag	Silver
$Ag-Pd$	Silver-Palladium
$Ag-Pt$	Silver-Platinum
Na_2O_3	Sodium Carbonate
W	Tungsten

Résumé

Introduction

Les fréquences millimétriques ont été initialement utilisées pour des applications militaires et spatiales. Aujourd'hui, l'utilisation de ces fréquences prend un grand intérêt pour les applications commercials afin d'obtenir une bande passante plus large en fréquence et ainsi un débit d'information plus élevé. En même temps, les demandes de miniaturisation ont conduit à une évolution des technologies d'intégration vers l'utilisation de modules multi puce en 3D. Ces évolutions nécessitent la mise au point de technologies innovantes et performantes, contribuant à de nouvelles voies d'intégration de différents éléments dans un même module et à la conception de nouvelles topologies de dispositifs et systèmes complets 3D.

Récemment, l'utilisation de la technologie LTCC est devenue très populaire dans tous les secteurs de l'industrie électronique tels que les communications sans fil, l'automobile, le militaire, l'avionique, l'espace, et d'autres applications du fait de la densité d'intégration élevée qu'elle permet, de ses faibles pertes et de sa fiabilité. Cette technologie offre une grande flexibilité dans la réalisation de boîtiers hyperfréquences avec la possibilité d'intégrer des dispositifs passifs tels que inductances, condensateurs, filtres et résonateurs à l'intérieur du substrat tandis que les composants actifs sont montés en surface du boîtier ou dans des cavités.

La Figure 1 montre une coupe transversale d'un système en LTCC qui est essentiellement structuré en 3D à partir de feuilles en céramique-verre laminées ensemble et cuites en une seule étape. Ces feuilles connues aussi sous forme crue par GREEN-TAPES sont découpées individuellement en formes carrées puis percées à l'aide d'un laser. Des cavités ou d'autres formes complexes peuvent être créées dans cette étape. Les trous sont métallisés pour assurer l'interconnexion verticale entre les couches. Ces trous sont remplis et les différentes lignes de transmission sont déposées par sérigraphie sur chaque couche. Ensuite, les couches sont empilées et pressées pour en faire une structure en 3D. Finalement, le circuit est cuit selon un profil défini jusqu'à 850 $^{\circ}C$ pour avoir un seul bloc. Le procédé de cuisson conduit à un circuit qui est rétréci de 0.1 à 18 % dans les directions x et y, et de 15 à 40 % dans la direction z.

Les objectifs en terme de recherche et développement dans cette thèse peuvent se regrouper en trois axes :

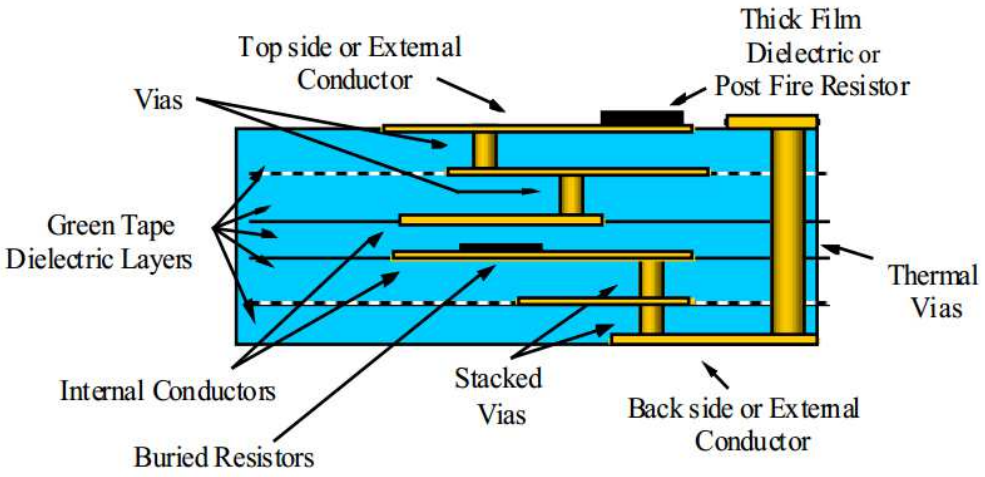


Figure 1: Coupe transversale d'un circuit en LTCC

1. La partie technologique dédiée à la mise en place de la technologie LTCC au laboratoire Lab-STICC à Telecom Bretagne et qui a pour but de choisir les matériaux en LTCC convenables pour nos applications, de valider le procédé de fabrication des circuits multicouches en LTCC, de trouver les différentes tolérances mécaniques et hyperfréquences liées à cette technologie et finalement de mettre en place des règles de conception pour réaliser ce type de circuits.

2. La partie RF qui valide la technologie LTCC dans les bandes de fréquences RF. Cette validation est réalisée en utilisant des structures simples telles que des lignes de transmission et résonateurs planaires pour extraire en particulier les propriétés diélectriques du substrat en LTCC.

3. Le projet "mm-Packaging" qui a pour objectif de concevoir, réaliser et caractériser des boîtiers multicouches en LTCC intégrant de circuits intégrés monolithiques micro-ondes MMIC (en anglais "'Microwave Monolitic Integrated Circuits"), des transitions et des dispositifs passifs dans un même module. Ce projet a été réalisé en collaboration avec le département Micro-Technologie et Nanoscience de l'université CHALMERS (Göteborg, Suède) qui est spécialisé dans la conception et la fabrication de puces MMIC en bande millimétrique et submillimétrique.

Mise en place de la technologie LTCC

Cette partie vise à introduire et développer LTCC comme une nouvelle technologie au département Micro-ondes de TELECOM BRETAGNE, afin de permettre la réalisation de modules RF à haute performance et à taille réduite. La mise en place de la technologie LTCC consiste tout d'abord à choisir les matériaux, à valider le procédé de fabrication, à résoudre des différentes problèmes technologiques rencontrées lors de la validation et finalement à mettre en place des règles de conception.

Choix des matériaux

Le premier critère à considérer avant de commencer toute conception des circuits hyperfréquences concerne le choix des matériaux à utiliser. Aujourd'hui, plusieurs fabricants (Dupont, Ferro, Heraeus, Kyocera...) sont sur le marché et proposent leur propre substrat en LTCC. Les propriétés physiques et électriques (permittivité, pertes diélectriques, épaisseur des couches, conductivité thermique,...) des matériaux pour le LTCC varient selon leur composition. Le Tableau 1 présente les principales caractéristiques de quelques exemples de matériaux en LTCC disponibles sur le marché.

Table 1: Caractéristiques principales de quelque matériaux en LTCC

Propriété	**DuPont 951**	**Ferro A6M**	**ESL 41010**	**ESL 41110**	**Heraeus CT2000**
Permittivité	7.8	5.9	7.4	4.2	9.1
Pertes diélectriques	0.0015	< 0.002	< 0.005	< 0.004	< 0.002
TCE ($ppm/°C$)	5.8	7.5	7	6.4	5.6
Conductivité thermique ($W/m.°K$)	3	2	$2.5-3$	$2.5-3$	3
Retrait $x-y$ (%)	12.7	15	13	15	10.6
	± 0.3	± 0.2	± 0.5	± 1	± 0.5
Retrait z (%)	15	25	17	16	16
	± 0.5	± 0.5	± 1	± 2	± 1.5

Pour nos applications, le substrat ESL41110 a été sélectionné du fait de sa faible valeur de permittivité par rapport aux autres matériaux. Cette valeur nous permet de travailler avec des lignes 50 Ω plus larges et ainsi réduire la complexité de fabrication lors de la sérigraphie des conducteurs. De plus, elle permet de minimiser les effets de couplage entre les différents éléments du circuit. Finalement, la faible valeur de permittivité du substrat choisi permet d'éviter l'excitation des modes supérieurs à des fréquences très élevées. Un autre substrat de permittivité 18 a été aussi sélectionné pour créer des fonctions de découplage capacitif. D'autre part, l'or ESL802 est utilisé comme matériau conducteur pour le remplissage des vias et l'or ESL803 pour le dépôt des conducteurs (lignes, plans de masse,...). Le matériau fugitif ESL49000 est utilisé pour le remplissage des cavités lors du pressage.

Procédé de fabrication

Après le choix des matériaux nécessaires, l'étape suivante consiste à définir, vérifier et valider les étapes de fabrication de circuits en LTCC. Cette validation est faite par une série de circuits réalisés en utilisant les moyens disponibles dans le laboratoire. Nous rappelons que le procédé de fabrication LTCC (Figure 2) consist en préparation des couches, poinçonnage des vias et des cavités, remplissage des vias par une pâte conductrice, sérigraphie des conducteurs, empilement des couches, pressage, cuisson, et finalement mesure et validation.

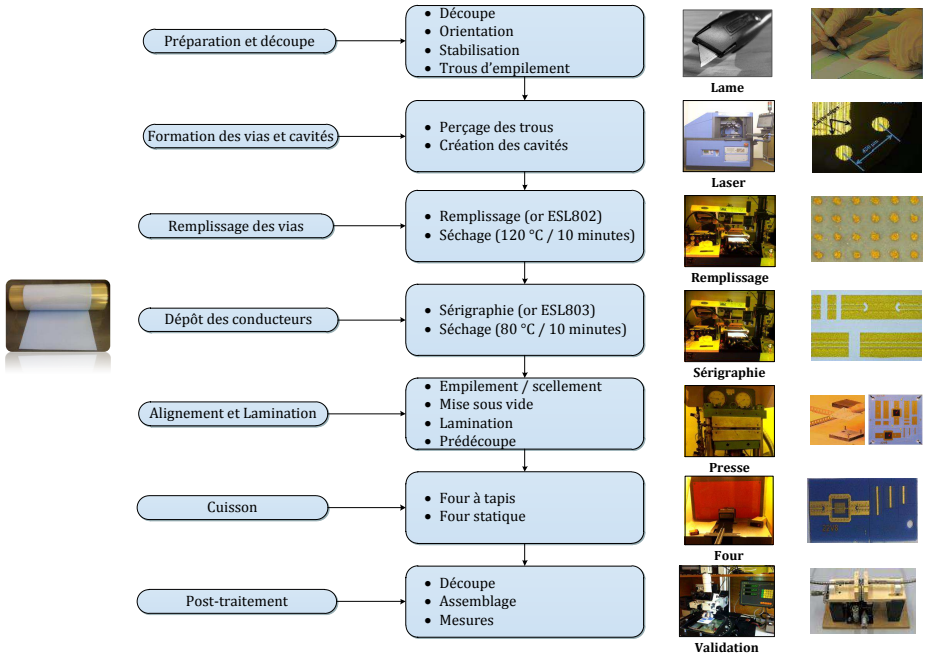


Figure 2: Procédé de fabrication des circuits en LTCC à Telecom Bretagne

Préparation des couches

Souvent, les bandes en LTCC sont délivrées sous forme d'un rouleau. Les couches sont tout d'abord découpées à l'aide d'une lame avec une dimension de 2" × 2". Une marque d'orientation est créée pour la rotation des couches de 90° lors de l'empilement afin de compenser le retrait du substrat lors de la cuisson dans toutes les directions. Ensuite, les couches sont stabilisées à 80°C pendant 30 minutes pour faire relaxer les couches. Finalement, les trous nécessaires pour l'empilement sont créés à l'aide du Laser.

Perçage des trous

Après la préparation des couches, les trous nécessaires pour l'interconnexion électrique et la dissipation thermique sont créés à l'aide de notre laser Nd-Yag ASTREE 250. Les paramètres du laser en termes de puissance et de vitesse de déplacement sont ajustés. Des trous jusqu'à 150 μm de diamètre peuvent être percés, des cavités et des formes complexes peuvent être aussi découpés.

Remplissage des trous

Une fois que les trous sont percés, l'étape suivante concerne le remplissage des trous par une pâte conductrice. Ce procédé est réalisé par la machine de sérigraphie standard en utilisant

un écran maillé. Après la préparation de l'écran, les paramètres de la machine en terme de vitesse de la raclette, d'alignement et de distance écran substrat sont réglés. Ensuite, les trous sont remplis par l'or ESL802 et sont finalement, séchés après remplissage à 120 $^{\circ}C$ pendant 10 minutes.

Sérigraphie

Après le remplissage des trous nécessaires pour la création des interconnexions verticales entre les couches, les lignes horizontales sont ensuite déposé par sérigraphie sur chaque couche à travers un écran maillé et en utilisant l'or ESL803. La largeur et l'espacement des conducteurs minimaux obtenus sont de 120 μm. Après sérigraphie, le séchage des lignes est réalisé à 80 $^{\circ}C$ pendant 10 minutes.

Alignement et empilement

Les différentes couches LTCC sont empilées manuellement dans l'ordre en utilisant un support mécanique nécessaire pour l'empilement. Ensuite, les couches sont collées et mis sous vide afin d'évacuer l'air localisé entre les couches.

Lamination

Après empilement, les couches sont laminées à 200 bars, à 70$^{\circ}C$ pendant 10 minutes en utilisant une presse uniaxiale. Le matériau fugitif ESL49000 est utilisé afin d'éviter l'écrasement des cavités pendant la lamination. Après lamination une prédécoupe avec une lame chauffante jusqu'à la moitié de l'épaisseur du circuit peut être réalisée. Cette prédécoupe permet de casser manuellement les différents éléments du circuit après cuisson.

Cuisson

La cuisson de notre circuit en LTCC est établie en utilisant deux fours : un four à tapis ou un four statique. Le four à tapis consiste à placer le circuit sur un tapis qui traverse des zones préchauffées tandis que dans le four statique le circuit est placé dans le four et la température varie selon un profil de cuisson défini. La plupart de nos circuits en LTCC sont cuits dans le four statique. Le profil de cuisson comporte trois phases : la phase de "burn-out" qui commence par une montée de la température jusqu'à 450$^{\circ}C$ suivie d'une fixation pendant 2 heures. A la fin de cette étape tous les éléments organiques sont éliminés. Ensuite, la phase de cuisson qui débute par une montée de température jusqu'à 850$^{\circ}C$ suivie par un arrêt de 15 minutes. A la fin de cette phase, le circuit devient solide et prend ses dimensions réelles après le retrait du substrat en x, y et z. Finalement, le circuit est refroidi jusqu'à la température ambiante.

Post-traitement

Après cuisson, des étapes secondaires destinées à la découpe, mesure et validation. Les circuits en LTCC prédécoupés après lamination sont découpés manuellement. Ensuite, une mesure dimensionnelle en surface est réalisée à l'aide d'un microscope 3D tandis que les éléments internes du circuit sont inspectés et mesurés après enrobage à froid. Finalement, l'assemblage et le montage des puces et des connecteurs sont effectués.

Problèmes technologiques

Lors de la validation du procédé de fabrication, nous avons rencontré plusieurs problèmes technologiques qui sont liés aux diffèrents paramètres de chaque étape de fabrication. Ces problèmes (Figure 3) sont tout d'abord identifiés, analysés et finalemet des solutions sont proposées afin d'obtenir des conditions de fabrication optimales pour chaque étape.

Figure 3: Solutions proposées pour les diffèrents problèmes technologiques rencontrés lors de la validation du procédé de fabrication

Règles de conception

Après la validation du procédé de fabrication des circuits en LTCC, nous avons mis en place des règles de conception qui permettent d'aider les utilisateurs de cette technologie à Telecom Bretagne pour toute conception de modules multicouches en LTCC. Ces règles qui sont regroupées dans un document détaillé contiennent les dimensions physiques nécessaires pour concevoir ce type de circuits en utilisant les matériaux LTCC provenant du fabricant Americain ESL. Elles sont basées sur les propriétés des matériaux et les équipements de

fabrication disponibles dans le laboratoire. La Figure 4 montre une vue de coupe d'un circuit en LTCC avec les différents éléments nécessaires pour la conception des circuits multicouches en LTCC.

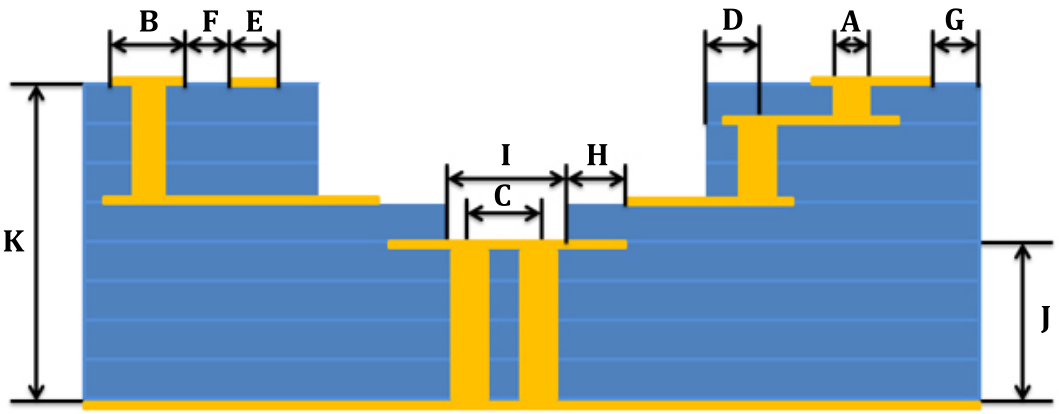


Figure 4: Vue en coupe d'un circuit en LTCC avec les différents éléments nécessaires pour la conception des boîtiers en LTCC

Les valeurs dimensionnelles des différents éléments sont illustrées dans le Tableau 2. Ces valeurs sont exprimées dans le système METRIC et sont données pour un circuit après cuisson.

Table 2: Les dimensions minimales des différents éléments d'un circuit en LTCC package

Element	Carécteristique	Dimension
A	Diamètre du trou	150 μm
B	Plot du trou	*Diamètre du trou* + 50 μm
C	Espacement entre trous	3 × *Diamètre du trou*
D	Distance trou-périphérie du substrat	2 × *Diamètre du trou*
E	Largeur de la ligne	105 μm
F	Espacement entre deux lignes	105 μm
G	Distance ligne-périphérie du substrat	200 μm
H	Distance ligne-périphérie de la cavité	200 μm
I	Largeur de la cavité	1.8 mm
J	Epaisseur de la cavité	300 μm
K	Epaisseur du substrat	450 μm

Validation RF de la technologie LTCC

Après la validation de la technologie LTCC en termes de conception et de fabrication, cette technologie a été validée dans les bandes de fréquences RF afin de réaliser des boîtiers hyper-fréquences multicouches en LTCC. Dans cette partie, nous présentons tout d'abord l'extraction

des paramètres électriques du substrat ESL41110 jusqu'à 40 GHz en utilisant des lignes de transmission et des structures résonnantes planaires. Finalement, le projet MM-PACKAGING qui a pour but d'intégrer des puces VCO dans des boitiers multicouches en LTCC est présenté.

Lignes de transmission

Les lignes de transmission sont utilisées dans les circuits hyperfréquences pour interconnecter les différents éléments actifs et passifs du circuit. Le choix de la topologie de la ligne (micro-ruban, coplanaire, coplanaire avec un plan de masse,...) est essentiel car il affecte la performance du circuit. Dans cette partie, nous présentons la conception, fabrication et caractérisation d'une ligne micro-ruban et d'une ligne coplanaire avec un plan de masse en dessous. La ligne coplanaire est exclue de notre étude à cause de difficultés de fabrication.

La ligne micro-ruban conçue en 50 Ω est implémentée sur six couches du substrat ESL41110 de permittivité 4,2. L'épaisseur du circuit est de 450 μm et la largeur de la ligne est de 880 μm. D'autre part, la ligne coplanaire avec un plan de masse en dessous est implémentée sur huit couches du substrat ESL41110. La largeur de la ligne centrale est de 600 μm et la dimension de la fente est de 120 μm. L'épaisseur du substrat est de 600 μm. Après réalisation de ces lignes en utilisant le procédé de fabrication mis en oeuvre, nous avons eu une tolérance de fabrication de $\pm 10 \mu m$. La mesure de deux lignes est effectuée à l'aide de l'analyseur de réseau ANRITSU 37397C et la cellule de mesure développée au laboratoire (voir Figure 3.23-(b)). Cette cellule intègre des connecteurs SOUTHWEST qui fonctionnent jusqu'à 40 GHz. Un calibrage SOLT est réalisé au niveau des connecteurs à cause du problème de reproductibilité du contact lors du calibrage TRL. Les résultats de simulation, mesure et retro-simulation sont illustrés dans la Figure 5. La mesure et la rétro-simulation incluent les effets des connecteurs coaxiaux de la cellule.

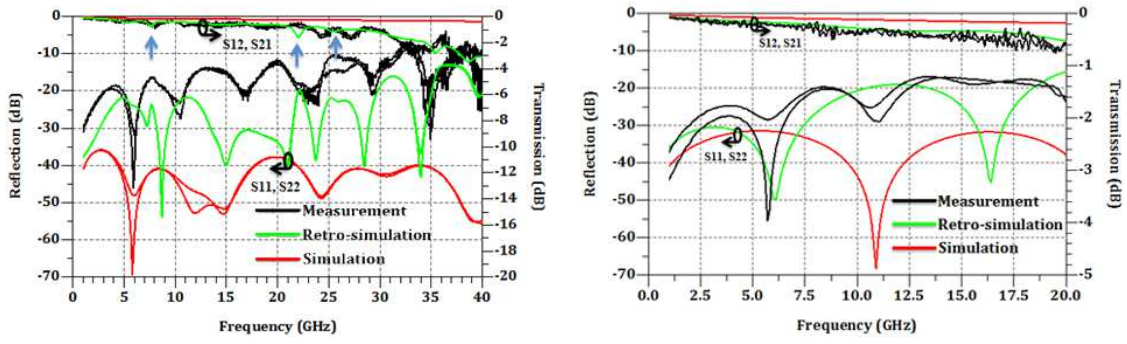


Figure 5: Simulation, mesure and retro-simulation des lignes de transmission : (a) Ligne micro-ruban. (b) Ligne coplanaire avec un plan de masse en dessous

Les résultats de mesure sont adaptés à ceux de la rétro-simulation en termes de transmission et réflexion. Pour la ligne micro-ruban, la réflexion est meilleure que 10 dB, et les pertes de transmission sont de l'ordre de 1.5 dB à 30 GHz tandis que pour la ligne coplanaire la

réflexion est meilleure que 18 dB, et les pertes de transmission sont de l'ordre de 0.8 dB à 20 GHz

Résonateurs

Les quatre résonateurs (deux en anneaux et deux en T) présentés dans cette section sont implémentés sur six couches ESL41110. Les résonateurs nommés "Ring 1" et "T1" sont simulés jusqu'à 26 GHz et sont conçus pour être mesurés à l'aide des connecteurs SMP montés en surface. Les autres nommés "Ring 2" et "T2" sont simulés jusqu'à 40 GHz et sont mesurés dans la cellule avec des connecteurs SOUTHWSET. L'épaisseur du substrat est de 450 μm. En supposant une constante diélectrique de 4.2, la largeur de la ligne micro-ruban est de 880 μm pour une impédance caractéristique de 50 Ω. Le Tableau 3 donne les dimensions des résonateurs conçus.

Table 3: Dimensions des résonators micro-rubans

Paramètre	**Ring 1**	**Ring 2**
r_{mean}	5 mm	2.6 mm
L_{ring}	31.5 mm	16.335 mm
g_{ring}	120 μm	450 μm
	T1	**T2**
L_{stub}	8 mm	4 mm

Les résultats de simulation, mesure et retro-simulation (pour "Ring2" et "T2") de résonateurs réalisés sont représentés dans la Figure 3.27 et la Figure 3.29. Ensuite, l'extraction de la constante diélectrique du substrat ESL41110 est effectuée aux fréquences de résonance mesurées. La Figure 6 donne la valeur de la constante diélectrique obtenue par les différents résonateurs.

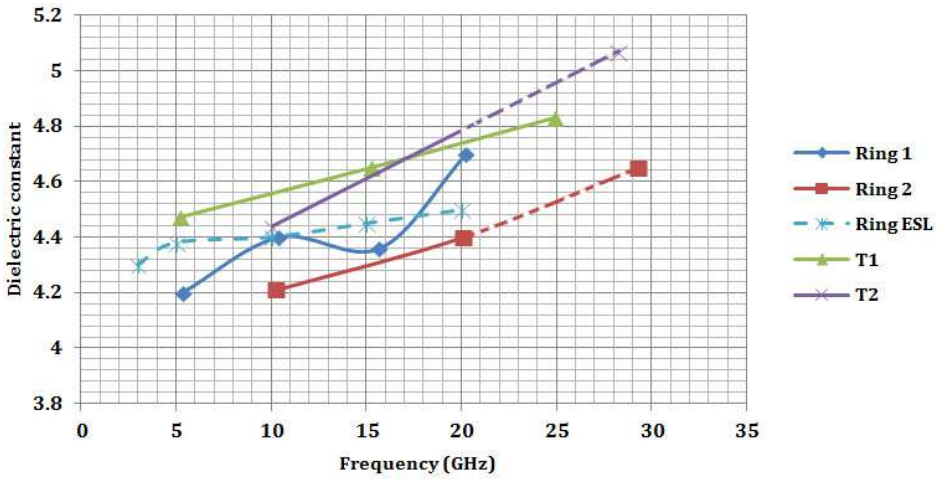


Figure 6: Constante diélectrique à partir de différentes méthodes de mesure

Projet mm-Packaging

Le projet commun avec l'université de CHALMERS, MM-PACKAGING, consiste à concevoir, réaliser et valider d'un boîtier en technologie multicouche LTCC intégrant un circuit oscillateur en technologie MMIC. Cet oscillateur possède une bande de fonctionnement en fréquence de 2 GHz (10.6-12.6 GHz). Il comporte une sortie RF et quatre entrées DC (base, collecteur et varactor).

Le boîtier conçu est composé de huit couches de substrat ESL41110. L'interconnexion entre la puce MMIC et le boîtier est effectuée par des fils d'or (Wire Bonds) de diamètre 25 μm. La puce est placée au niveau de la quatrième couche dans une cavité pour minimiser la longueur des fils. Afin de délivrer la puissance maximale de la puce vers le boîtier et éliminer les effets parasites indésirables des interconnexions, un réseau d'adaptation semi-localisé est réalisé au niveau de la connexion des fils d'or. Le signal de sortie de l'oscillateur est ramené en surface du boîtier grâce à une transition coplanaire vers une ligne strip-line à travers une interconnexion semi-coaxiale sur quatre couches. Cette interconnexion est optimisée par le placement de vias métallisés autour du signal pour obtenir une impédance de 50 Ω. L'objectif de cette transition est de pouvoir utiliser un connecteur SMP monté en surface. Les trous métallisés assurent la connexion entre les différents plans de masse du boîtier. La Figure 7 représente le boîtier final incluant la sortie RF ainsi que les entrées DC de la puce MMIC. L'alliage or-platine (en gris) est utilisé pour la soudure des connecteurs.

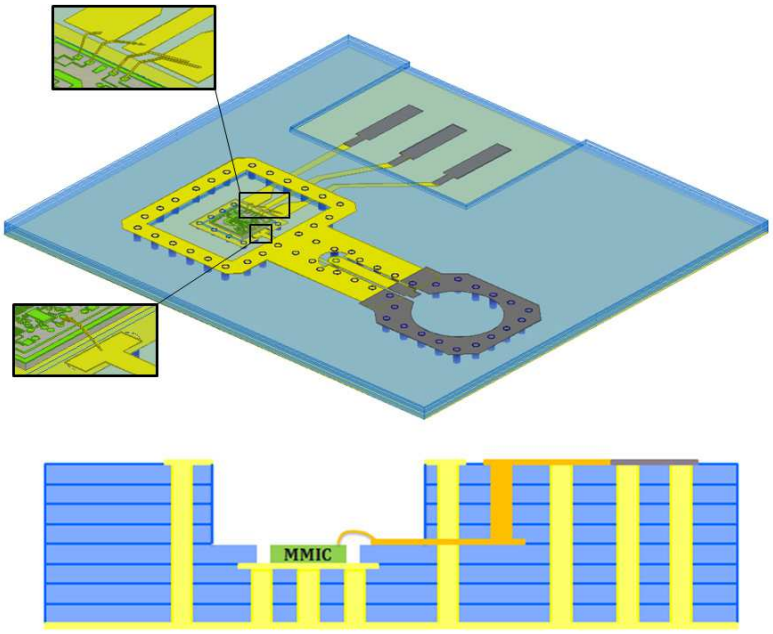
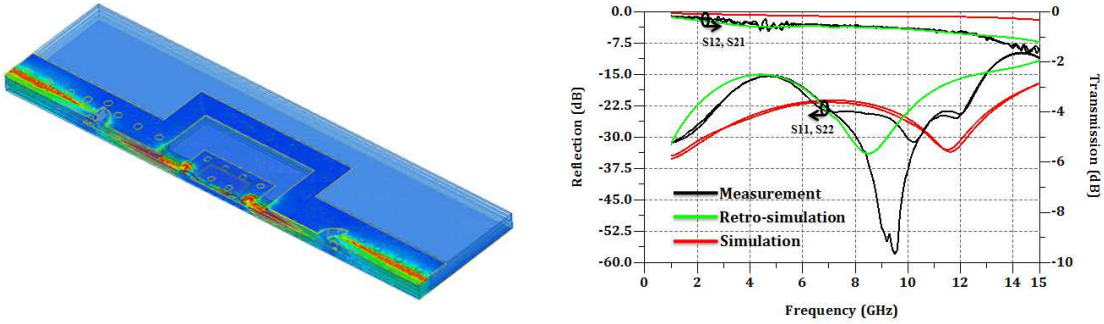


Figure 7: Vues 3D et en coupe des huit couches ESL41110 du boîtier LTCC pour le VCO MMIC

Avant la réalisation finale du boitier représentée dans la Figure ci-dessus, et afin de la valider en termes de paramètres S, la partie RF est simulée et fabriquée tout d'abord en configuration back-to-back pour caractériser les différentes transitions. Après cuisson, les différentes parties

du circuit sont découpées au niveau des accès des transitions et les fils d'or sont interconnectés. La mesure en paramètres S est réalisée entre 1 et 15 GHz en utilisant l'analyseur de réseau ANRITSU 37397C à l'aide de la cellule de mesure.

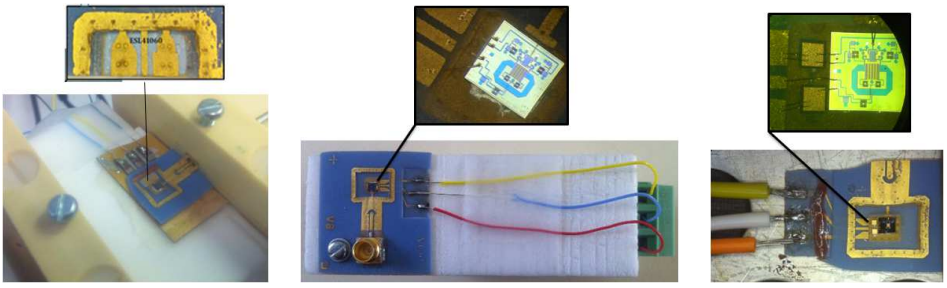
Les résultats de mesure et rétro-simulation montrent un coefficient de réflexion meilleur que $-20\ dB$ entre 10.6 et 12.6 GHz. Les pertes en transmission (S12 et S21) mesurées à 12 GHz sont de l'ordre de 0.75 dB, incluant les pertes dans les connecteurs.



(a) (b)

Figure 8: Validation des transitions RF du boîtier: (a) Champs E à 11 GHz. (b) Paramètres S

Après la validation de la partie RF, le boîtier final de l'oscillateur MMIC a été fabriqué. Ce boîtier inclut les accès DC destinés à l'alimentation de la puce MMIC. Trois prototypes différents ont été conçus et fabriqués en utilisant le procédé de fabrication LTCC décrit précédemment afin d'y intégrer les capacités de découplage sur les accès DC (en plus du découplage sur la puce). Le premier prototype n'intègre aucune capacité, le deuxième permet le report de capacités CMS et pour le dernier, des capacités MIM (Métal-Isolant-Métal) sont intégrées à l'intérieur du substrat. Le matériau diélectrique ESL41060 à haute permittivité (environ 18) est utilisé pour l'isolant. La valeur des capacités réalisées est de l'ordre de 2 pF.



(a) (b) (c)

Figure 9: Boîtiers final en LTCC: (a) Avec capacités MIM intégrées. (b) Sans capacités de découplage. (c) Avec capacités SMD

La mesure de la bande d'accord et de la puissance des oscillateurs mis en boîtiers est réalisée à l'aide de l'analyseur de spectre ROHDE & SCHWARZ FSQ (20 $Hz - 40\ GHz$). La tension de base (Vb) de l'oscillateur est de 2.77 V, la tension du collecteur est fixée à 5 V ($Ic = 35\ mA$) et

la tension du varactor est variable entre 0 et 14 V.

La Figure 10 présente la bande de fréquence mesurée en fonction de la tension du varactor pour deux prototypes (sans capacité et MIM) réalisés. La fréquence de l'oscillateur après la mise en boîtier varie entre 10.2 et 12.6 GHz. La puissance de sortie mesurée varie entre -2.4 et -1.2 dBm sur toute la bande de fréquence mesurée.

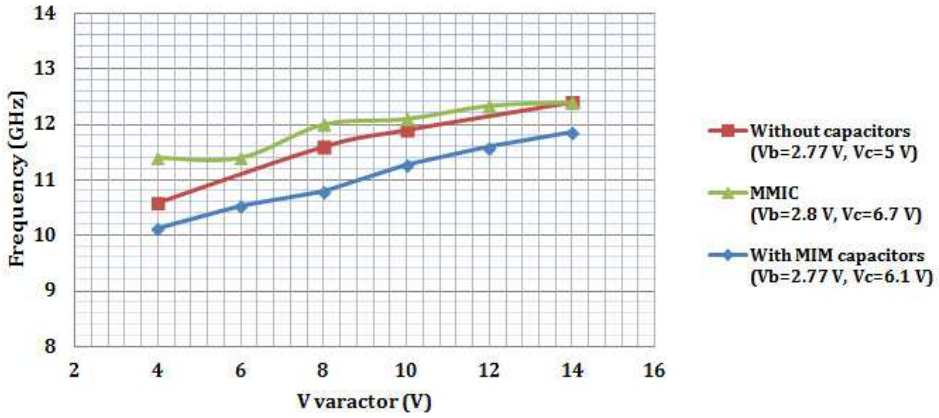


Figure 10: Mesure de la bande de fréquence d'accord des oscillateurs en puces et en boîtier LTCC

Conclusion

Les activités de recherche dans cette thèse ont été concentrées dans deux directions : technologique concernant la mise en place de la technologie LTCC au laboratoire LAB-STICC de TELECOM BRETAGNE et le projet MM-PACKAGING qui a pour but d'intégrer de circuits intégrés micro-ondes MMIC dans des boîtiers multicouches en LTCC.

Au niveau technologique, nous avons tout d'abord sélectionné les matériaux convenables pour nos applications tenant en compte les aspects de fabrication et de la performance. Ensuite, nous avons validé la technologie LTCC en utilisant les moyens disponible dans le laboratoire. Les différents problèmes technologiques rencontrés lors de cette validation sont aussi résolus. Finalement, des règles de conception ont été mises en place pour aider les utilisateurs de la technologie LTCC à TELECOM BRETAGNE de concevoir leur circuit en LTCC.

Au niveau du projet MM-PACKAGING, nous avons réalisés trois boîtiers en fonction de découplage sur l'alimentation DC et intégrant un oscillateur MMIC en puce fonctionnant dans une bande de fréquence de 2 GHz entre 10.6 and 12.6 GHz. Ces boitiers ont été conçus, fabriqués et mesurés.

Introduction

Today, the microwave domain, that was initially confined to military use, opens its doors for commercial applications such as mobile phones and wireless communication systems. Constraints are not exactly the same, the efficiency and compactness are needed but for high-volume consumer products, manufacturing costs, design delays, and maintaining the optimal electrical performance are strongly required. The current trend is therefore to leave the conventional packaging technologies with discrete components where the performance is degraded due to the important loss of interconnections and replace it with more and more advanced packaging technologies that integrate all functions of a microwave communication module on the same substrate. The aims of this is to improve the compactness of the system, reduce the fabrication costs and optimize the interconnect performances.

Another trend for microwave systems comes with an increasing operating frequency, which now reaches the millimeter and sub-millimeter wave range, in order to obtain higher data rates and larger frequency bands. This increase in frequency accompanied by a decrease in wavelength and a reduction in circuit dimensions requires high density packaging technologies.

In the past years, various packaging technologies with organic and ceramic based materials have been reported for microwave and millimeter wave circuits. Ceramic substrate materials are the best choice for Radio Frequency (RF) packaging applications due to its good electrical, mechanical and thermal properties at very high frequencies. Today, the LTCC technology that combines the low loss dielectric materials and high conductivity metalizations becomes very popular for RF packaging applications due to its multilayer capability. LTCC technology is nearly used in all electronic sectors such as telecommunication, automotive, medical and military.

This Ph.D thesis aims at the integration of millimeter wave integrated circuits in LTCC packages thanks to a research project in collaboration with CHALMERS UNIVERSITY OF TECHNOLOGY, Göteborg, Sweden. The LTCC technology is introduced and developed at LABSTICC/TELECOM BRETAGNE in order to produce ultra-miniature, low cost and high performance RF packages and modules. The manufacturing process of LTCC technology is first validated and the design rules are then implemented. Finally, the LTCC technology is validated in the RF bands up to 40 GHz.

This thesis is arranged as follows:

Chapter 1 describes the current state of the art of packaging technologies in the RF domain. The evolution as well as the packaging technologies classification followed by the assembly techniques is presented. The main features, evolution and materials characteristics of LTCC technology are also reviewed. Next, the motivation of LTCC choice for RF packaging applications has been demonstrated and finally, the recent packaged Microwave Monolithic Integrated Circuits (MMICs) in LTCC technology are presented.

Chapter 2 that is dedicated to the technological part of LTCC technology illustrates, the choice of LTCC materials and the manufacturing process validation using available equipments in the laboratory. The different encountered problems during validation are investigated and the proposed solutions are also presented. The LTCC DESIGN RULES needed for future LTCC designers at TELECOM BRETAGNE is presented at the end of this chapter.

Chapter 3 details the RF validation of LTCC technology up to 40 GHz using simple RF structures such as planar transmission lines and resonators. The study starts from theoretical point to the measurement results via circuit simulations and fabrication. The last part presents the design, fabrication and characterization of multilayer LTCC packages for MMIC integration.

Chapter 1

Introduction to RF packaging technology

Contents

Introduction

Initially, microwave frequencies have been used mostly for military and space applications. Today, the need of greater bandwidth and higher data rates have resulted in increasing interest in the use of microwave and millimeter wave frequencies in commercial applications such as mobile phones, wireless communications and automotive radar systems. At the same time, the demand for low cost, high volume and miniaturized circuit fabrication has led to an evolution in integration technologies. This evolution is moving towards three dimensional (3D) packaging technologies. One of the most viable packaging technologies to satisfy these demands is the *Low Temperature Co-fired Ceramic* (LTCC), which is a multilayer technology that has been widely used in wireless communication, automotive, military, medical, space and several other applications. This technology offers great potential in fabrication of 3D packages because it enables vias and passive components to be integrated inside the substrate whereas, the active devices can be mounted on the top of package.

This chapter describes the current state of the art of packaging technologies in the RF domain. Section 1.1 present status and trends of packaging technologies up to millimeter wave frequencies. Then, the evolution and packaging technology classification followed by the assembly techniques are overviewed. Section 1.2 focuses on the main features of LTCC, which is the selected technology for our packaging applications. The LTCC evolution and material properties are also reviewed. Next, a more detailed description on RF characteristics of LTCC technology is given in section 1.3. The LTCC technology is thus demonstrated as an advanced solution for packaging applications in the microwave frequency ranges. Some recent packaged MMIC chips in LTCC technology are described in section 1.4, and finally, the objectives of this thesis are presented in section 1.5.

1.1 RF packaging: an evolution towards SiP technology

Today, microwave products invade our daily life with an increased use in many areas such as communication, scientific and commercial applications. As shown in Figure 1.1 from ITRS [1] [1], the development of new microwave systems is characterized by the need of higher performance, smaller size, lower power, lower cost and multi-functional systems. These characteristics cannot be met with conventional packaging and interconnect technologies because there are limitations in interconnect density, thermal management, bandwidth and signal integrity. System-in-Package (SiP) (section 1.1.6.2) is perhaps the most important technology to address these limitations.

In this section, we will give some background on RF packaging. After defining packaging, we discuss challenges and issues of several factors that influence the electrical, thermal and mechanical behavior of the RF package. Next, evolution of integration technology from Single Chip Package (SCP) to SiP through Multi Chip Module (MCM) (section 1.1.6.1) is reviewed.

[1] INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

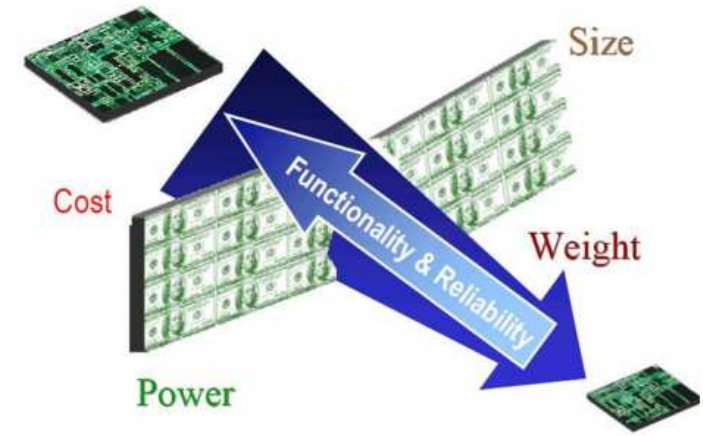


Figure 1.1: The market demands of microwave system production

Finally, the current assembly techniques at the chip level are discussed.

1.1.1 Radio Frequency

The frequencies falling between 3 MHz and 300 GHz are called *Radio Frequencies*. The term *Microwave* refers to the frequencies between 300 MHz and 300 GHz that are electromagnetic waves with wavelengths ranging from 1 m to 1 mm. The microwave frequencies are divided in operational bands. Table 1.1 shows frequency range and free space wavelength with letter designation of each band from 1 to 300 GHz. We note also that the *millimeter wave* range start at about 30 GHz.

Table 1.1: Standard Radio-Frequency Letter Band Nomenclature[2]

Band	**Frequency Range**	**Wavelength**
	GHz	**mm**
L Band	1 – 2	300 – 150
S band	2 – 4	150 – 75
C band	4 – 8	75 – 38
X band	8 – 12	38 – 25
Ku band	12 – 18	25 – 17
K band	18 – 27	17 – 11
Ka band	27 – 40	11 – 7.5
V Band	40 – 75	7.5 – 4
W band	75 – 110	4 – 2.4
mm band	110 – 300	2.4 – 1

1.1.2 Definition of packaging

The term *packaging* is defined as a way to enclosure and protect a product for distribution, storage and use [3]. In microelectronics, this term has a meaning somewhat different and may be defined as a discipline whose objective is to integrate one or several Integrated Circuits (ICs) in one system. The traditional role of a package is to serve as a protective mechanical enclosure; with the market growth of microwave systems, the advanced package has been transformed into a sophisticated thermal and electrical management platform [4].

1.1.3 Interest of packaging

To understand the importance of RF packaging, it is necessary to think of the package in terms of a system. Normally, a RF system is composed of several elementary functions such as frequency generation, amplification, mixing, filtering, etc. These elementary functions may be integrated on one semiconductor chip thanks to MMIC technology [5, 6]. However, monolithic integration of these functions on a single chip implies that the integrated circuit becomes extremely complex and may be specific to one single application. Moreover, additional constraints appear particularly in the dimensions of the chip which is very thin, difficult to use and handle.

Another approach, offering more flexibility consists of placing and interconnecting the IC (or MMIC) in a package; it is possible to speak of SCP [7, 8] for one IC (or Chip Scale Packaging (CSP)) and MCM for several ICs. This approach (Figure 1.2) offers more flexibility than integration on chip described above because the level of functionality is achieved at the package and not only at the chip.

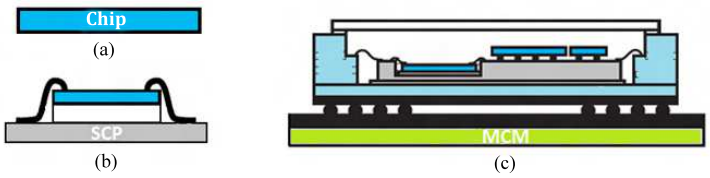


Figure 1.2: Integration possibility of microwave functions: (a) Unpackaged chip. (b) Single Chip Package. (c) Multi Chip Module

1.1.4 RF Packaging: challenges and issues

Packaging at microwave and millimeter wave frequencies comes with the same challenges as packaging at lower frequencies. Furthermore, the complexity of the package increases with frequency, because the circuit features have dimensions that are in the same order as the wavelength. In this case, the package type will be selected according to the performance and cost. For some applications, such as space, we promote the performance of the package such as the hermeticity, reliability, environmental endurance and redundancy. For others, usually

consumer high-volume products, we will tend to minimize the cost. Beyond the cost, the package becomes part of the circuit and strongly affects reliability and electrical performance of the system [9]. In order to minimize the effect of the package on the MMIC performance, different factors such as electrical, material, mechanical and thermal properties must be considered during the design and fabrication process as shown in Figure 1.3.

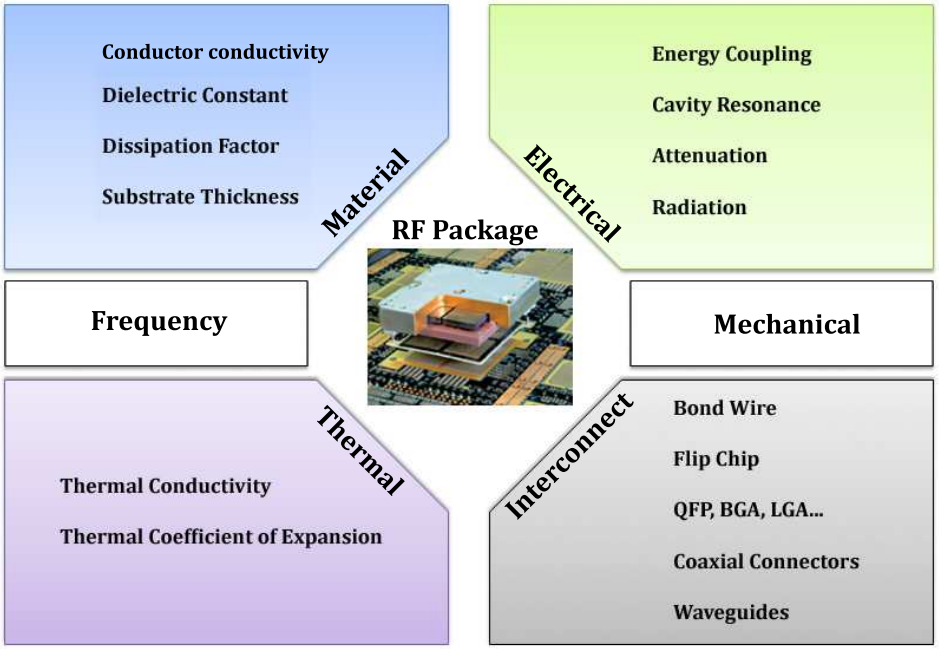


Figure 1.3: Factors that must be considered during the design of an RF package

The design of an RF package must address three parts: RF signal, Direct Current (DC) bias and cavities. RF signal is the most critical part that will affect the electrical performance. The electrical performance of a package is determined by the level of signal integrity that it maintains for signal transmission, from the chip to the board. For instance, a MMIC within a package must be connected to the module; the most frequently used method is the wire bonding method. However, at microwave frequencies, a wire bond behaves as an inductor and at millimeter-wave frequencies it can even act as an antenna or resonator. Other major difficulties, at high frequencies, are energy coupling between adjacent traces, attenuation due to losses, cavity resonances over the operating frequency range and radiation.

Substrate material selection is another important part of the packaging at high frequencies because material proprieties will affect the impedance and insertion losses of transmission lines. Normally, there are two main families of substrate products: organic and ceramic materials. The choice of the substrate material is based on various criteria such as the packaging technology (Printed Circuit Board (PCB), thick film, thin film ...), the electrical constraints that are related to the application, mechanical and thermal constraints that are related to the environment and of course to the cost which is very important for the manufacturer.

The main features of a dielectric substrate are:

- Dielectric constant or relative permittivity, ε_r
- Dissipation factor or loss tangent, $tan\,\delta$
- Thermal Coefficient of Expansion, TCE $(ppm/^\circ C)$
- Thermal conductivity $(W/m.^\circ K)$

The dielectric constant affects the dimensions and impedance of transmission lines. A substrate having a high dielectric constant will reduce radiation losses and decrease the size of circuit while a low dielectric constant will minimize coupling and provide better isolation between parts of the package. In addition to the material itself, the thickness of the substrate should also be taken into account. A thin substrate results in a suppression of higher order propagation modes, reduces radiation losses and minimizes the circuit size.

The insertion losses of a circuit are related to the dielectric substrate. Low loss circuit requires a dielectric substrate having a dissipation factor as low as possible. We also note that the insertion losses are related to the metallic conductor's loss through the conductivity of the used metallization (Cu, Ag, Au ...).

Another essential concern that must to take into account in packaging is the thermal performance. Thermal conductivity is a significant factor in the choice of materials. This is especially a very important factor in the case of RF power amplifiers which can have high power densities. For reliable direct attachment of die, the TCE of the substrate materials must be matched to the semiconductor materials such as Silicon (Si) and Gallium Arsenide (GaAs).

1.1.5 Levels of packaging

RF packaging can be performed at several levels; the number of levels is related to the final product. Normally, MMICs can be packaged at three levels [6]; these levels that represent the manufacturing process of microwave systems are shown in Figure 1.4. Each level of packaging has an interconnection device associated with it.

Microwave packaging levels are summarized in the following points:

- Level 1: Active and passive component interconnections on a monolithic semiconductor chip, wire bonding and flip chip assembly techniques
- Level 2: Packaging of semiconductor chips into SCP, Dual-In-Line Packages (DIPs), Small Outline Integrated Circuits (SOICs), Ball Grid Array (BGA), Land Grid Array (LGA), Quad Flat Package (QFP) ....
- Level 3: MCM, SiP using surface mount techniques, coaxial connectors, waveguides ...

- Level 4: Microwave module, PCB, Board to Board connections ...

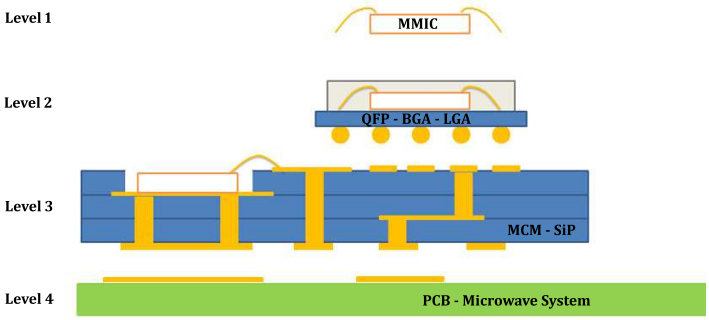


Figure 1.4: From IC to functional microwave system: interconnection techniques and packaging levels of MMICs

1.1.6 Evolution

In order to meet the market demands in terms of size, performance and multi-functional of microwave systems, the packaging technology has evolved the last decades from SCP toward MCM technologies. However, the implementation of active and passive devices in an MCM is still a significant development axis in regards of microwave and millimeter wave functions.

The current trend is to obtain High Density Integration (HDI) multi-functional modules. As shown in the Figure 1.5 from UMS SEMICONDUCTOR [10], the integration technologies are today moved towards 3D MCM and SiP technologies. This concept allows integrating several technologies in a single system. The vertical interconnections drastically minimize the input-output count of the circuit, improve the compactness of the system and then increase the desired operating frequency.

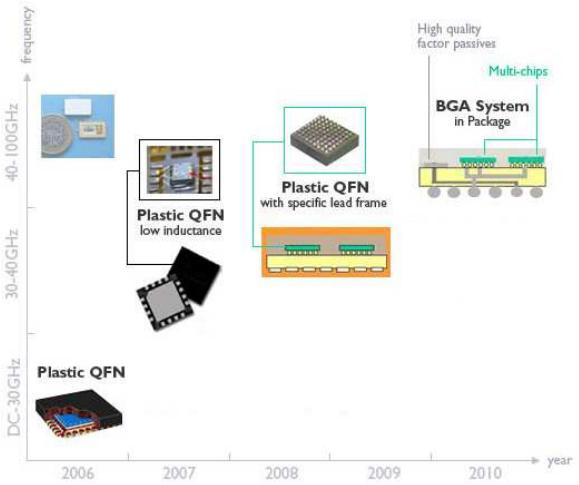


Figure 1.5: Packaging roadmap: Evolution toward SiP technology

In this section, we briefly present the current packaging technologies used up to microwave and millimeter wave frequencies. The advantages and disadvantages of each technology are also reviewed.

1.1.6.1 Multi Chip Module

MCM technology, which has been presented in [11, 12, 13, 14], means the implementation of various functions on the same board. This board can be a single or a multilayer circuit, where different signals, such as DC and RF, are routed. An MCM module is a hybrid circuit, which can contain different families of technologies and components. In addition, this technology allows better integration of components in comparison with a discrete and planar integration; this integration means that all the functions are installed on one substrate layer.

Several commercially available technologies have been developed to fabricate MCMs. These technologies are based on different manufacturing processes and are divided into three groups using the base materials as shown in Figure 1.6: MCM-L for laminate substrate, MCM-D for deposition and MCM-C for ceramic materials.

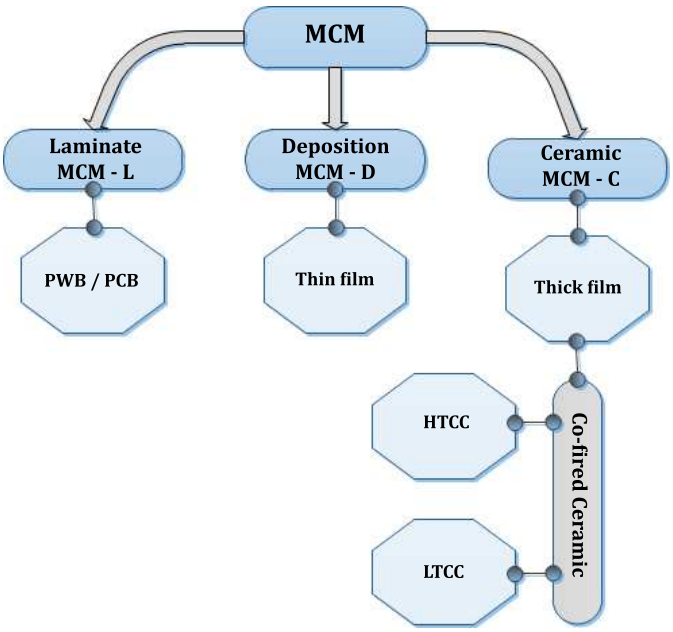


Figure 1.6: Available commercial MCM technologies

MCM-L The laminate substrate is normally an organic material and can be used to create multi-layer structures. The MCM-L is fabricated using Printed Wiring Board (PWB) methods. This technology allows high density integration and can be characterized by a simple manufacturing process and low cost materials with a dielectric constant that varies from 2 to 10. However, the main drawbacks of some organic materials such as FR4 are that they do not allow good thermal performance and are frequency limited (Appendix A).

MCM-D The MCM Deposited, also known as thin film technology, is fabricated by depositing conductor material and etching with a photo-lithography method. The metal trace widths and gaps can be smaller than 20 μm resulting in an excellent performance especially at microwave and millimeter wave frequency. Dielectric Thin film can be created using silicon nitride or polyimide to realize capacitor and metal crossovers.

MCM-C There are three variants that are commonly used for MCM Ceramics technologies: thick film and co-fired ceramics that include HTCC and LTCC. Thick film modules are fabricated by starting with a ceramic base material that is already fired while co-fired ceramics are fabricated with unfired green tape layers, which are fired after processing at high temperature.

Thick film The thick film materials can be Alumina (Al_2O_3), Aluminum Nitride (AlN) or Beryllia (BeO). The ceramic substrate is laser drilled to produce via holes. Next, screen printing technique is applied to the substrate to create metal conductors. Resistors, dielectrics or additional metal layers can also be printed and fired. Depending on the substrate materials, thick film technology has good performance at microwave and millimeter frequencies, but the integration density is relatively low when compared to multilayer board, because this technology enables only one level of layer.

Co-fired Ceramics Co-fired ceramic packages are fabricated through two distinct processing stages that include material preparation and green tape processing. Material preparation consists of mixing ceramic powder or glass-ceramic material in order to form a dielectric green tape. Green tape processing consists of punching cavities, via punch, via fill, screen printing, lamination, firing, additional printing, sawing and brazing. Figure 1.7 from ADTECH CERAMICS [15] shows the fabrication processing flow of co-fired ceramic technologies.

HTCC In High Temperature Co-fired Ceramic (HTCC), Alumina and Aluminum Nitride materials are a good choice for hermetic packaging and are most commonly used in military and aerospace, radar, medical devices and high temperature applications. The major benefits of HTCC are good electrical performances at microwave frequencies, good metal adhesion to substrate, high mechanical strength and good thermal conductivity ($20-25\ W/m.^\circ K$) (Appendix A). The main drawback of HTCC ceramic is that the firing temperature is very high ($1200-1800^\circ C$). This imposes the choice of metals such as Molybdenum (Mo) or Tungsten (W) which unfortunately suffer from important resistive losses as compared to gold and silver metallization.

LTCC Another co-fired ceramic is the LTCC technology which is processed in the same way as HTCC. LTCC allows the use of noble conductors such as gold and silver with a good electrical performance at microwave and millimeter wave frequencies. LTCC enables the use of high dielectric and ferromagnetic tapes for capacitors and inductors realization respectively. The main drawbacks of LTCC are the low thermal conductivity ($2-4\ W/m.^\circ K$) of the substrate

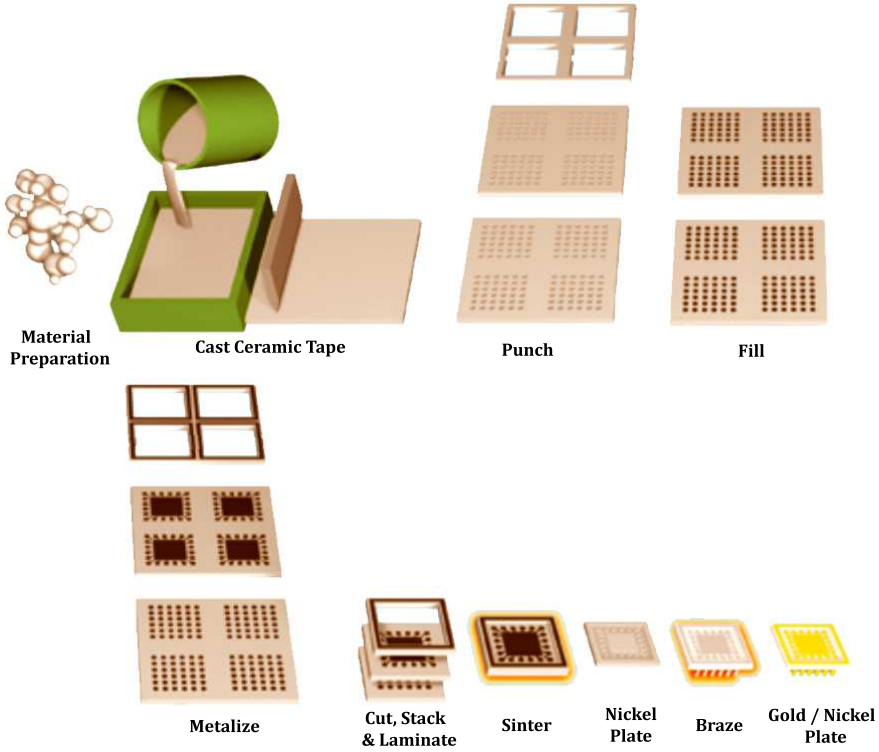


Figure 1.7: Fabrication process of co-fired ceramic technologies

materials, the complex manufacturing process, and the important dimensional tolerances due to the shrinkage of substrate during the firing process.

1.1.6.2 System in Package

The current trend in RF packaging is to integrate maximum functionalities in the same miniaturized system. The driving force of this is economical, because integrating different technologies in one system saves space and reduces cost. To achieve these goals, the integration method called System in Package [1, 16, 17] must be taken into account (Figure 1.8).

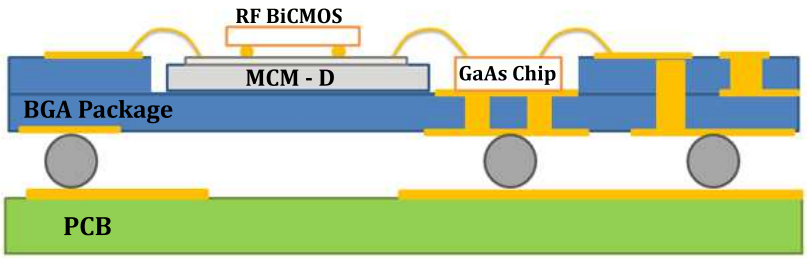


Figure 1.8: An example of System in Package

The ITRS defines SiP as *"a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, Micro Electro Mechanical Systems (MEMS), optical components and other packages and devices"* [1].

This concept is an extension of MCM that appeared in the 1980*s*. The SiP is more than an integrated circuit package containing several chips. Components of SiP technology are fully functional systems or subsystems when compared to a standard package. They contain one or more active devices traditionally placed on the top of the package. According to the chosen integration technologies, passive components may be integrated in some cases inside the substrate and a 3D integration method can be used. 3D integration can save significant volume and space compared to planar integration. The complete 3D integration offers advantages of compactness, and weight reduction. The lengths of interconnections are reduced, which allows a reduction in propagation time and parasitic effects. In addition, due to the circuit size and interconnect count reduction, 3D integration should allow a reduction in consumption, and ultimately lower cost. But 3D integration presents significant constraints in some cases. The increase in integration density leads to increased power density and complicates thermal conditioning.

1.1.7 Assembly technologies

The general process of preparing an integrated circuit starts with the integration of circuits in some semiconductor materials. Then, the chips are tested to identify functional chips and failed chips are marked. After dicing, the semiconductor chips are assembled in a package to ensure their role in a system or micro-system. The first level (chip to package) assembly technologies are wire bonding, flip chip and Tape Automated Bonding (TAB). These interconnect techniques are designed to provide the electrical connection between the chip and the package.

This section focuses on the assembly technique at the chip level. Only, the wire bonding and flip chip techniques are discussed, the TAB technique is not presented here because it is suitable for dies having large numbers of input-output and is not used for RF and microwave dies having a small number of pad connections.

1.1.7.1 Wire bonding

Wire bonding is the oldest interconnection technique used in the electronics industry. Over 95% of the high volume packages are produced using wire bonding technique [18]. With this method the chip is glued or soldered to a substrate with the circuit face directed upwardly. The connection to the package by wire bonding is generally made using ultrasonic and thermo-compression techniques.

The basic principle is to connect two pads together using a conductive wire. There are several

types of wire bonding amongst which the wedge and ball bonding are the most frequently used in hybrid manufacturing; the *wedge bonding* which is an unidirectional technique and the *ball bonding* that connects the chips in all directions. Figure 1.9 shows the geometrical parameters of a bond wire. Geometrical and structural variables include the type of the bond (Wedge or Ball), the diameter of the wire, the height of the bond loop and the distance between the bond pads. The bond wire materials are discussed in [19]. Gold, Aluminum and Copper (for high-volume production) are the metals used in wire bonding. Beyond its high electrical conductivity that is important for RF applications, the special benefits of gold wire include its resistance to corrosion and, especially, the relative ease with which it can be bonded into position by both thermo-compression and ultrasonic techniques. Copper is rarely used and only in extremely high-volume production.

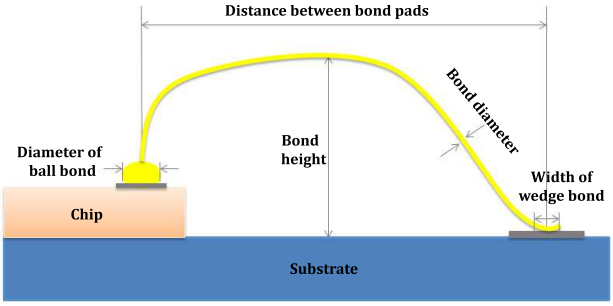


Figure 1.9: Geometry of bond wire (Ball and wedge)

Wire bonding (wedge or ball) is still dominant in the RF domain especially for frequencies up to 10 GHz. At microwave and millimeter wave frequencies the characteristic impedance of wire bond becomes higher and the wire bond behaves as an inductor. To optimize the performance of insertion loss and return loss of a bond wire in microwave frequency range, it is recommended to reduce the wire length by placing the chip in a cavity in order to reduce the inductance of the wire bond and by using multiple wire bonds or ribbon bonding. In [20], the results of an evaluation of wire bonding in terms of wire length up to 94 GHz is presented.

Wedge bonding *Wedge bonding* is performed with the ultrasonic method using vibration and pressure. For microwave applications, gold wires are used generally. Figure 1.10 shows the process steps of this method. The wire is first connected to the chip pad and then to the second contact pad on the substrate, finally the wire is cut.

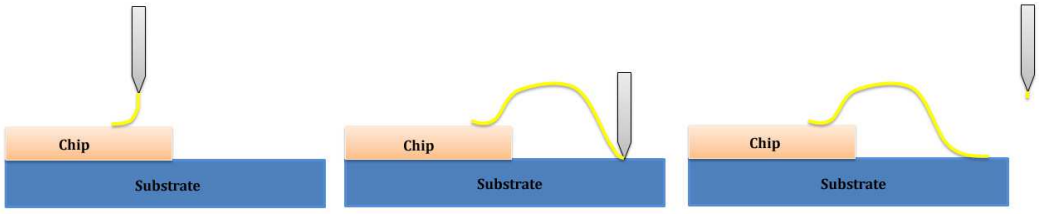


Figure 1.10: Wedge bonding process

Ball bonding Figure 1.11 shows the principle of the *ball bonding* process. This technique uses more frequently a gold wire in order to interconnect the chip to the substrate. The wire bonding is normally performed at temperatures between 100 to 200°C. The last step is dedicated to the formation of a gold ball. First ball is bonded on the chip pad. Then, the wire is moved to perform a second bond formation on the substrate and then the wire is cut and finally a new ball is formed.

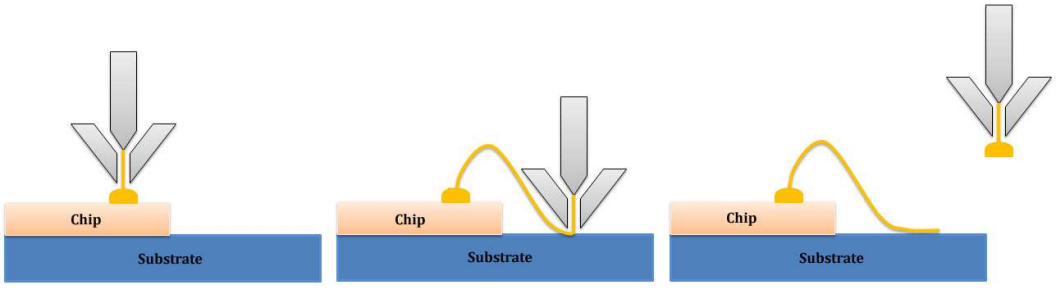


Figure 1.11: Ball bonding process

1.1.7.2 Flip chip

Flip chip bonding is an interconnection technique in which the die is turned upside down and connected to the substrate. This method was initially developed by IBM [2] and then known as $C4$ (Controlled Collapse Chip Connection), thereafter several variants of the flip chip method have been developed to accommodate for different requirements. The flip chip method allows better performance in the RF devices when compared to the wire bonding because the interconnection length between the bare chip and the substrate is reduced and then a low parasitic inductance is achieved. In addition, this method can significantly increase the number of connections count compared to bonding and increase the integration density of circuits.

The principle of flip chip method consists in depositing conductor materials on the chip pads, generally solder bumps. The chip is then returned (flip chip) and soldered to substrate. The bumps are the only mechanical contact between the chip and the package. After solder re-flow, the connection between the chip and the substrate is established. In addition, to reduce the thermo-mechanical constraints an under-fill resin can be used to fill the space between the chip and the substrate. Figure 1.12 shows an example of flip chip connection using solder bumps and the under-fill between the chip and the substrate.

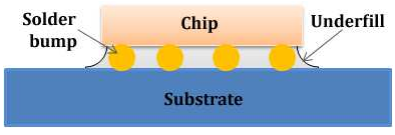


Figure 1.12: Flip chip interconnect geometry

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1.2 LTCC technology

As discussed in section 1.1.4 and section 1.1.6, the substrate material is a fundamental element of any microwave package. In recent years, research in ceramic materials has seen a growing interest for RF packaging applications. Ceramic materials have been used for several decades to make RF filters, resonators, antennas and others RF circuit boards in hybrid modules. The development of new technologies has been, and still is, driven by the need for increased interconnection density, better electrical performances and smaller circuit size. Evolved from thick film and HTCC technologies, a new ceramic technology has emerged these last twenty years called *LTCC*.

This section gives a general overview of LTCC technology, from its historic evolvement to the substrate material processing and properties, advantages of this technology are also presented. The manufacturing process of LTCC circuits is discussed in chapter 2.

1.2.1 Definition

LTCC, that stands for *Low Temperature Co-fired Ceramics*, is a multilayer technology that is used in nearly all types of electronic applications (Figure 1.13), such as automotive industry, consumer electronics, wireless, telecommunication, military, avionics, space, medical and other applications [21, 22].

Figure 1.13: Wide range of LTCC applications (Sources: DT-MICROCIRCUITS [23], VIA ELECTRONICS [24] and IMST [25])

Figure 1.14 shows a cross section of an LTCC system which is basically a stack of thick-film ceramic sheets. LTCC sheets also know as GREEN TAPE^{TM} (named from DUPONT^{TM}) in its unfired form are individually cut, drilled and screen printed, then stacked and laminated

before the firing below 1000°C. The firing process leads to a mono-bloc circuit that is shrunk from 0.1 to 18 % in the $x-y$ direction, and from 15 to 40 % in z direction.

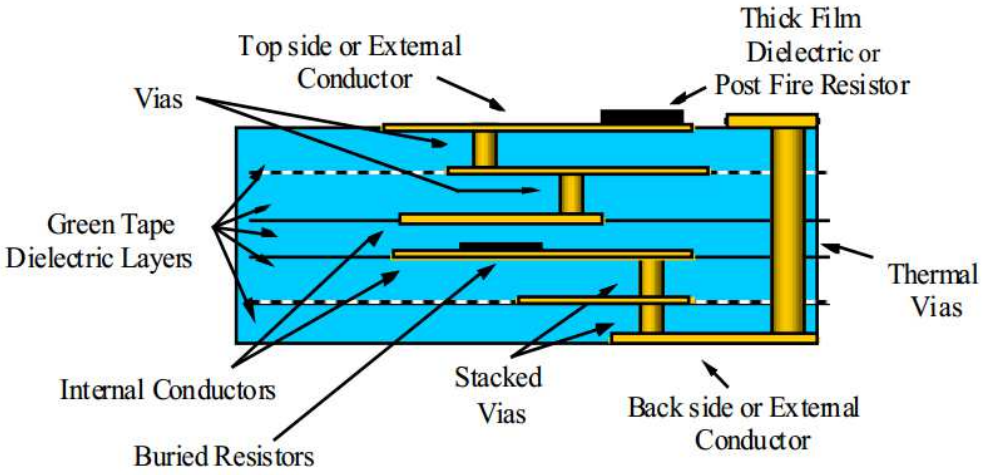

Figure 1.14: Cross section of LTCC module [26]

1.2.2 Evolution

Due to the great thermo-mechanical and electrical properties, ceramics have been used for more than 60 years for harsh environment applications such as aerospace, military, radar, automotive, and other applications. Today, ceramic materials are still the best choice for these applications, as well as for new applications such as wireless devices, MEMS and MMIC packages where there is a need for high electrical performance, high thermal stability and good mechanical strength. The co-fired ceramic substrate, which is processed as illustrated in the Figure 1.7, is normally composed of ceramic or ceramic-glass based materials.

The HTCC technology was born in the early 1950s for military applications. The base material of HTCC is usually Al_2O_3. Because of the high firing temperature of Al_2O_3, the conductor must have a high melting temperature. This type of material requires a firing temperature beyond 1600°C, and thus only high loss conductors such as Tungsten (W) and Molybdenum (Mo) may be employed. In the case of reliable and high performance devices at high frequencies, the conductors should exhibit high electrical conductivity, compatibility with other materials in the system, wire bond compatibility, good electrical and mechanical integrity and good adhesion to the substrate. For these reasons, and in order to avoid the drawbacks of HTCC technology, a new substrate material was developed in form of sheets in the middle of 1980s with firing temperature below 1000°C. As indicated by the name, the low temperature is the key feature of this technology because the low firing temperature allows the use of high conductivity metals with low melting point such as copper, gold and silver. Table 1.2 shows the HTCC and LTCC compatible conductors [27].

Table 1.2: The used conductors with HTCC and LTCC materials

Ceramic	Firing temperature ($^\circ C$)	Conductor	Melting point ($^\circ C$)	Conductivity (S/m)
HTCC	1600 to 1800	Mo	2610	1.87×10^7
		W	3410	1.815×10^7
		Mo-Mn	1246 – 1500	–
LTCC	900 to 1000	Cu	1083	5.8×10^7
		Au	1063	4.1×10^7
		Ag	960	6.17×10^7
		Ag-Pd	960 to 1555	–
		Ag-Pt	960 to 1186	–

1.2.3 LTCC materials

The LTCC materials have a higher percentage of glass and are often referred to as glass-ceramics [28]. From a general perspective, LTCC tapes are prepared by tape-casting [29] of glass-ceramic slurry on polymeric carriers using a doctor blade machine (Figure 1.15) varying the tape thickness between 50 and 400 μm.

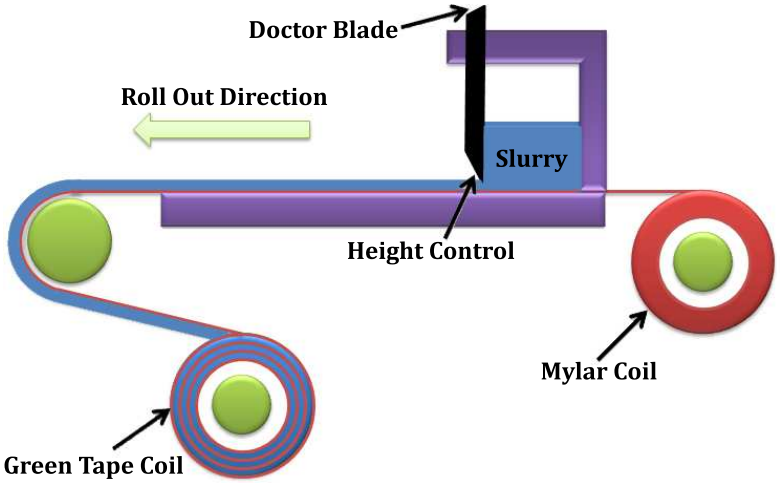

Figure 1.15: Tape casting process

The ceramic is usually Alumina (Al_2O_3), but it could be any other ceramic system, including high thermal conductive Beryllium Oxide (BeO), ferroelectric or ferromagnetic spinels [30]. Table 1.3 shows the base materials of LTCC substrate [31]. Glass is the key material of this mixture which reduces the firing temperature of ceramic material to about 850 $^\circ C$. A disadvantage of the presence of glass is that the substrate material provides inferior mechanical and thermal properties when compared to HTCC. Generally, the thermal conductivity of LTCC materials is about 2.5 to 4 $W/m.^\circ K$, which can, if necessary, be compensated with the use of thermal vias which increase the thermal conductivity up to about 50 $W/m.^\circ K$.

Table 1.3: LTCC substrate base materials

Base Materials	Composition
Cordierite	MgO, SiO_2, and Al_2O_3
Glass filled composite	SiO_2, B_2O_3, PbO, CaO, and Al_2O_3
Crystalline phase ceramics	B_2O_3, CaO, SiO_2, MgO, and Al_2O_3

Depending on the proportions of the glass ceramic compositions and other additional elements, the LTCC substrate manufacturers offer a wide range of dielectric tapes whose physical, electrical and thermo-mechanical properties vary: permittivity, dissipation factor, tape thickness, thermal conductivity, thermal coefficient of expansion, flexural strength, etc. As a result, one must select the material that best matches the requirements of a given application. Today, several LTCC manufacturers are present on the market (*e.g.* DUPONT [32], FERRO [33], ESL[3] [34], HERAEUS [35], ...) and proposing their own LTCC material. Table 1.4 lists the typical properties of major commercial LTCC tapes that are used for microwave applications.

Table 1.4: Typical commercial LTCC Tape Properties

Property	DuPont 951	DuPont 943	Ferro A6M	ESL 41010	ESL 41110	Heraeus CT2000	Heraeus HL2000
Dielectric constant	7.8	7.5	5.9	7.4	4.2	9.1	7.3
Loss tangent	0.0015	< 0.001	< 0.002	< 0.005	< 0.004	< 0.002	< 0.0026
TCE ($ppm/^\circ C$)	5.8	6	7.5	7	6.4	5.6	6.1
Thermal conductivity ($W/m.^\circ K$)	3	4.4	2	2.5 – 3	2.5 – 3	3	3
Density (g/cm^3)	3.1	3.2	2.5	3.16	2.3	2.45	2.9
Surface roughness (μm)	< 0.7	< 0.7	–	–	–	–	–
$x-y$ shrinkage (%)	12.7	9.5	15	13	15	10.6	0.16 – 0.24
	±0.3	±0.3	±0.2	±0.5	±1	±0.5	–
z shrinkage (%)	15	10	25	17	16	16	32
	±0.5	±0.5	±0.5	±1	±2	±1.5	–
Color	Blue	Blue	White	White	Blue	Blue	Blue

1.2.4 Advantages of LTCC technology

LTCC offers many benefits over other available technologies due to its multilayer capability and its high frequency characteristics. Numerous advantages can be listed such as:

- Low cost technology
- High integration density

[3] Electro Science Laboratory

- Low dielectric loss at high frequencies
- Buried passive elements (resistors, capacitors, inductances, etc)
- High thermal stability
- Good hermeticity
- Low thermal coefficient of expansion
- Complex shapes of substrate and cavities
- Various tape thickness
- Low resistivity conductor (Ag, Au ...)
- Good solderability and bondability
- Compatibility with a wide range of assembly techniques (wire bonding, flip chip, Surface Mount Technique (SMT), ...)

1.3 LTCC as a solution for RF packaging

The LTCC technology was originally developed in 1980s for military and medical applications. With the explosion of wireless technologies in middle of 1990s, the LTCC has become very popular for wireless and telecommunication products [36, 37] such as cellular mobile phones ($0.9-2\ GHz$), Global Positioning Systems (GPS) ($1.6\ GHz$), Wireless Local Area Network (WLAN)/Bluetooth ($2.4\ GHz$), broadband access connection systems ($5.8-40\ GHz$), millimeter wave communication systems ($60\ GHz$) [38, 39] and vehicle anti-collision radar ($77\ GHz$) [40].

The common requirements of such devices are good electrical performances especially, at high frequencies, high thermal and mechanical stability and, of course, low fabrication cost. Today, LTCC technology has attracted the attention of microwave engineers for RF packaging applications due to the excellent high frequency performance in terms of dielectric and conductors loss (up to $100\ GHz$), environmental conditions in terms of thermal stability and hermeticity, and finally the capability of integrating passive elements and fine line patterning that enables miniaturization and high packaging density.

As discussed in section 1.1.4, the electrical, thermal and mechanical material features strongly affect - beyond the design - the performance, size and reliability of RF packages. This section shows why LTCC is a good choice for RF and MMIC packaging applications. The high frequency characteristics, as well as, the electrical properties of LTCC materials are firstly discussed, and then the thermo-mechanical properties. Finally the passive integration, which is the main feature of LTCC technology, is also presented.

1.3.1 High frequency characteristics

The electrical properties of substrate materials are very important parameters for high-frequency applications. The LTCC substrate offers excellent electrical properties, and stability up to millimeter wave frequencies. The electrical parameters of substrate material include dielectric constant, dissipation factor and conductor loss.

1.3.1.1 Dielectric constant

The *dielectric constant* also called *relative permittivity* (ε_r) is the real part of the *complex permittivity* ($\epsilon = \epsilon' - j\,\epsilon''$) of the dielectric substrate. In high frequency electronic modules, different values of dielectric constant are advantageous depending on the application. For transmission lines (*e.g.* microstrip), a low dielectric constant is desired at microwave and millimeter wave frequencies to reduce capacitive effects between elements, and to avoid higher-order mode excitation (see section 2.1.1).

On the other hand, the wavelength λ of electromagnetic waves in the material (Equation1.1) is inversely proportional to the square root of the dielectric constant.

$$\lambda = \frac{c}{f\sqrt{\varepsilon_r}} \tag{1.1}$$

where c is the free-space velocity ($c \approx 3 \times 10^8\ m/s$), λ is the wavelength in m, and f is the frequency in Hz.

In this case, a high dielectric constant is beneficial in order to minimize circuit size such as filters, and other components. Furthermore, it is very important to use a very high dielectric constant to make decoupling capacitors [27].

The LTCC material offers a wide range of dielectric constants, because it depends on the proportion of glass material. Currently, commercial LTCC tapes exhibit ε_r (generally measured at 1 MHz) from 4 to 10 or more (Table 1.4). In addition, capacitive tape layers with high dielectric constant up to 300 can be found.

1.3.1.2 Dielectric Loss

The high frequency transmission loss is due to both dielectric and conductor loss ($\alpha = \alpha_c + \alpha_d$). The *dielectric loss* is related to the imaginary part of complex permittivity and is generally expressed in terms of the dissipation factor or loss tangent ($tan\,\delta$) [41]. We note that the conductor and dielectric loss are expressed according to the transmission line topology (section

3.1.1).

$$\tan\delta = -\frac{\epsilon'}{\epsilon''} \tag{1.2}$$

where ϵ' and ϵ'' are the real and imaginary parts of the complex permittivity respectively.

In RF applications, a low dissipation factor is desired to avoid excessive losses due to the dielectric substrate. The dissipation factor of LTCC materials varies from 0.001 to 0.006 (at 1 MHz) which is very low when compared to some organic materials.

1.3.1.3 Conductor loss

The other part of the total loss is due to the *conductor loss* (α_c). The conductor loss depends on the skin depth and surface roughness of the substrate. The *skin depth* (δ_s) represents the distance that the RF current penetrates into the conductor thickness. At low frequencies, the current is uniformly distributed within the conductor. As the frequency increases, the RF current concentrates on the surface part of conductor. This results in a conversion of RF energy into heat, and therefore increases the insertion loss. The relationship for skin depth is given by Equation 1.3 [41]

$$\delta_s = \frac{1}{\sqrt{\sigma\pi\mu f}} \tag{1.3}$$

where σ is the metal conductivity in (S/m), μ is the permeability of the metal ($\mu = \mu_r\mu_0$, $\mu_0 = 4\pi \times 10^{-7}$) and f is the frequency in (Hz).

As discussed in section 1.2.2, the low firing temperature of LTCC materials allows the use of noble conductors such as copper, silver and gold. These conductors have a higher conductivity than other metals.

It is also important to take into account the roughness of the conductor and dielectric which can increase the conductor loss at millimeter wave frequencies. The correction factor of attenuation due to the roughness is plotted in Figure 1.16. The new value of conductor loss is given by multiplying this factor by the calculated value of conductor loss without roughness as given in the following relation [42]

$$\alpha_c' = \alpha_c \underbrace{\left\{1 + \frac{1}{90} arctan\left[1.4\left(\frac{rgh}{\delta_s}\right)^2\right]\right\}}_{\text{roughness correction factor}} \tag{1.4}$$

The *roughness* (rgh) of LTCC material is about 0.33 μm, which falls between the 96 % Alumina,

which has a typical roughness of 0.44 μm, and the 99 % Alumina, which has a typical roughness of 0.1 μm [43].

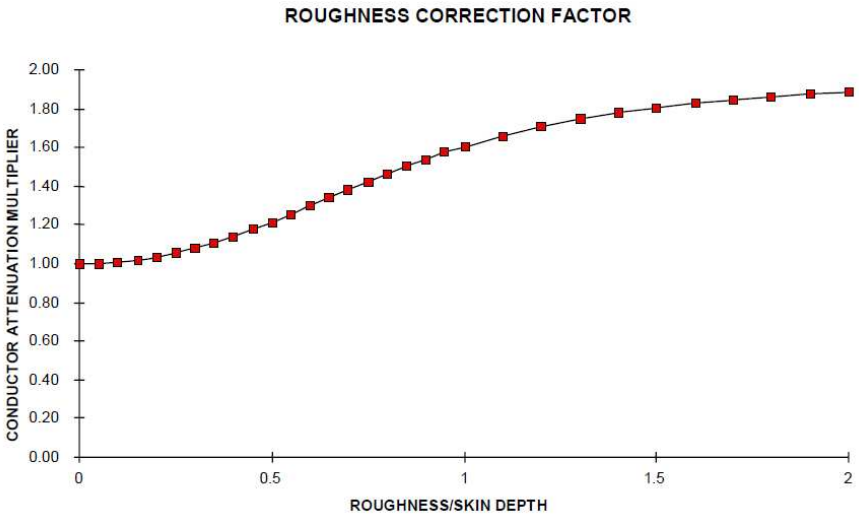

Figure 1.16: Conductor attenuation correction factor for roughness [43]

1.3.2 Thermo-mechanical properties

1.3.2.1 Thermal conductivity

In wireless and RF applications, the stability and uniformity of electrical properties over operating temperature ranges is critical. The thermal conductivity measures the ability of a material to conduct heat. The thermal conductivity value (2 to 4 $W/m.^\circ K$) of LTCC materials is far better than organic PCBs ($0.25-0.5 W/m.^\circ K$), but is relatively bad when compared to Alumina substrate ($20-25 W/m.^\circ K$). Thermal vias can be used to improve thermal conductivity of LTCC system (up to 50 $W/m.^\circ K$) [44].

1.3.2.2 Thermal coefficient of expansion

Thermal coefficient of expansion is an important parameter as it affects attached semiconductor chips. Therefore, the packaging substrate must exhibit a TCE value close to that of Si and GaAs $TCEs$ in order to avoid cracks in the die attach or interconnection rupture of flip chip or bond wire. The low TCE is also a great advantage of LTCC substrate which can vary between 5 and 7. Figure 1.17 illustrates the TCE of some semiconductors and substrate materials.

1.3.3 High density integration

LTCC technology is a good candidate for high density packaging needed for microwave and millimeter wave package miniaturization. Behind fine line patterning and small via diameter

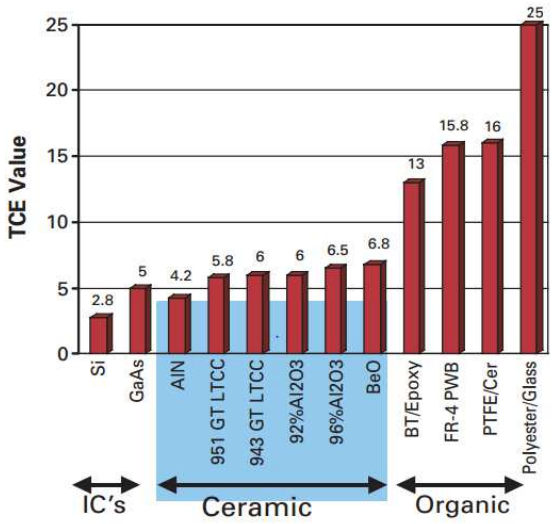

Figure 1.17: TCEs of some substrate and semiconductor materials [45]

and pitch required for high frequency design, the most important features of LTCC in terms of packaging density are passive integration and cavity formation.

1.3.3.1 Passive integration

One of the most attractive features of the LTCC technology is the ability to integrate passive elements inside the substrate (Figure 1.18). Passive elements include inductors, resistors, capacitors, LC shunts, LC series and other functionality components such as filters and resonators. Embedded passives provide high density integration, higher reliability through the reduction of number of inputs/outputs, and excellent performance through the reduction of interconnect counts. In addition, capacitive and magnetic tapes can be used to increase the value of integrated capacitors and inductors respectively.

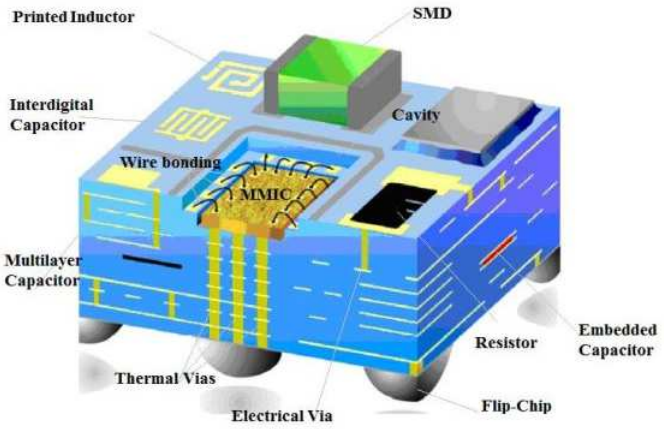

Figure 1.18: Passive components integration in LTCC substrate [46]

1.3.3.2 Cavities

Another capability of LTCC is the possibility to make cavities and 3D structures. Cavities can be used to interconnect semiconductor chips in order to decrease the length of the bond wires between the chip and the LTCC module; this is an essential concept at high frequencies because it reduces the parasitic inductance and improves the interconnect performance.

1.4 Recent applications

The LTCC technology is commonly used in four major product formats: component, integrated circuit package, functional MCM, and System in Package. As discussed in the previous section, the LTCC technology presents an excellent solution for RF applications and is being used in many GaAs MMIC packaging applications because of its closely matched TCE to that of GaAs (6.5 – 7). The challenge today with the growth of MMIC operating frequencies is to apply the LTCC technology at even higher frequencies going into millimeter wave and sub-millimeter wave range. Several LTCC studies have been conducted by research laboratories and industries up to millimeter wave range. The aim of this section is to present the recent state of the art of the LTCC use in millimeter wave packaging.

1.4.1 IMST

IMST[4] is specialized in the development of LTCC high-frequency modules for wireless and communication systems. These modules are usually composed of MMIC chips combined with embedded passive elements, transitions and other elementary functions. At the beginning of years 2000, several applications such as Frequency Modulated Continuous Wave (FMCW) automotive radar at 24 GHz [47], point to multi-point transceiver module at 26 GHz [48], packaged MMIC Low Noise Amplifier (LNA) and Multipliers up to 40 GHz [49] were published.

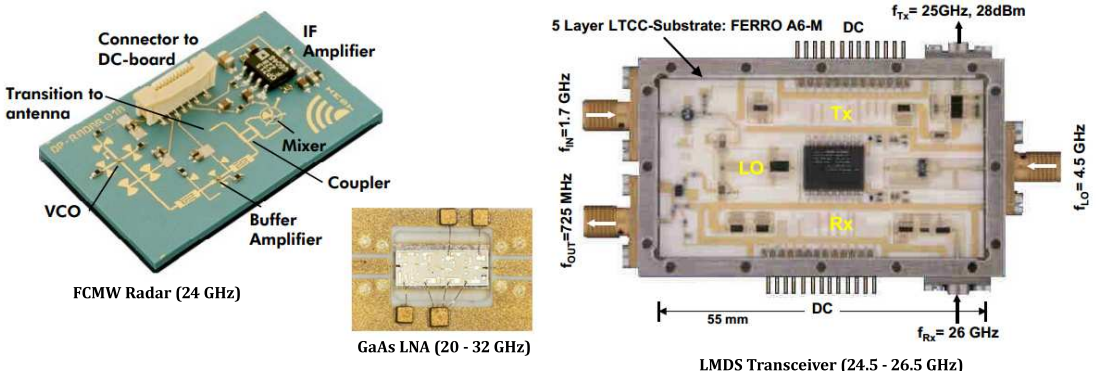

Figure 1.19: Some LTCC RF applications presented by IMST

Another application from IMST shown in Figure 1.20 represent a multilayer LTCC radar front-

[4] INSTITUTE FOR MOBILE AND SATELLITE COMMUNICATION TECHNOLOGY

end that was designed at 77 GHz. This LTCC front-end size is only $1.4 \times 30 \times 12$ mm including a broadband VIVALDI antenna [50].

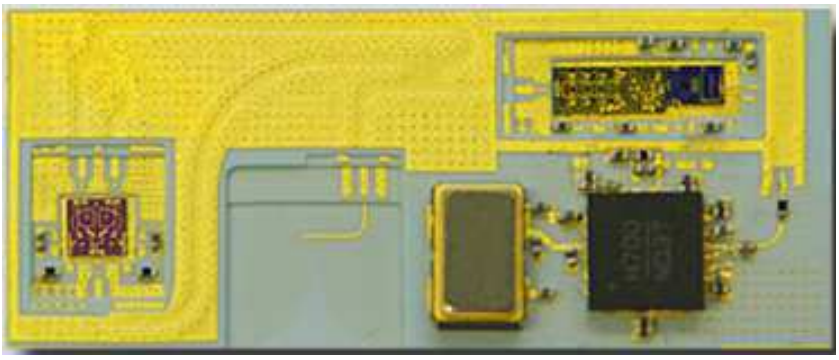

Figure 1.20: Photograph of 77 GHz radar front-end and antenna implemented on four DUPONT 9K7 LTCC layers (the dielectric constant of LTCC substrate is about 7, and the layer thickness is about 100 μm)

1.4.2 NEC

In [51] from KANSAI ELECTRONICS RESEARCH LABORATORIES - NEC[5], a 60 GHz band antenna integrated transmitter/receiver module in LTCC technology is presented. Figure 1.21 shows the photograph and structure of the module. A double slot antenna is printed on the LTCC substrate. The transmitter consists of an up-converter and an output amplifier. The receiver consists of an LNA and a down-converter. All MMIC chips are compatible with flip chip technology.

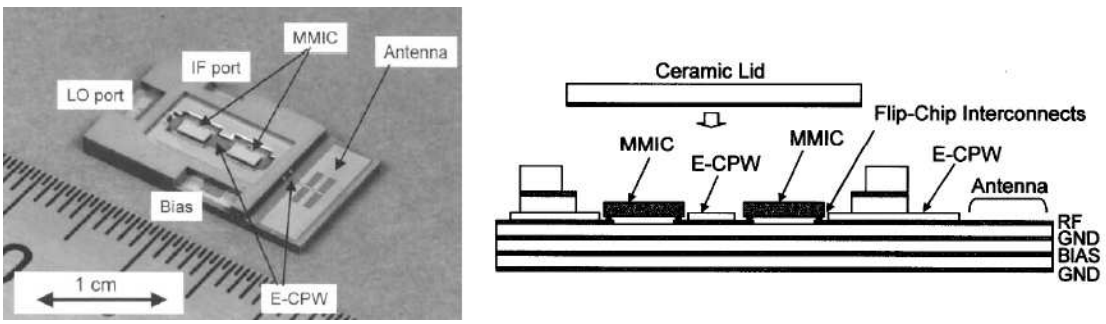

Figure 1.21: 60GHz-band antenna-integrated MCM using LTCC technology

Another application developed by NEC in LTCC for an MMIC functioning up to W-band was presented in [52]. The package structure includes a cavity for the flip chip MMIC and coplanar feedthroughs to improve radiation suppression.

[5] Nippon Electric Company

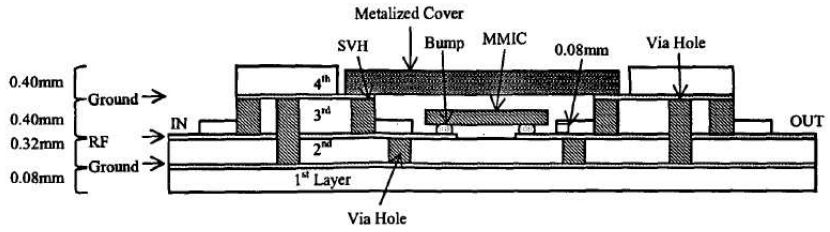

Figure 1.22: Cross sectional view of MMIC package in LTCC substarte

1.5 Objective of this thesis

Today, one of the cornerstones in microwave electronic system miniaturization is the System in Package. The main objective of this thesis is to study the LTCC technology to benefit the fabrication of miniaturized RF and microwave components and modules. The research activities in this Ph.D thesis can be grouped along two axes: the first one concerns the implementation and development of the "in-house" LTCC technology at the Microwave department of TELECOM BRETAGNE, while the second aims at packaging millimeter wave MMICs using LTCC thanks to a research project called "MM-PACKAGING" in collaboration with the Microwave electronics laboratory at CHALMERS UNIVERSITY OF TECHNOLOGY, Göteborg, Sweden.

According to these objectives, research and activities are outlined in the following order:

- Market study of the commercial LTCC tapes and substrate choice
- The equipments and techniques required to produce LTCC circuits
- LTCC process validation and resolution of technological problems
- Estimation of LTCC fabrication tolerances and "DESIGN RULES" definition
- Validation of LTCC technology in the RF bands
- MMIC packaging design, fabrication and characterization

Conclusion

Thanks to the complete study of the various packaging technologies used in the RF domains, the LTCC technology has been demonstrated in this chapter as a good solution for integration technique of different microwave functions. Its multilayer characteristics and high density integration capabilities make it an attractive candidate to meet the market needs in terms of miniaturization and SiP module integration. It presents indeed a good electrical performance up to millimeter wave frequencies and it is adapted to operate in harsh environmental conditions due to its thermo-mechanical characteristics.

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Chapter 2

Establishment of LTCC technology

Contents

Introduction

This chapter aims at introducing and developing LTCC as a new technology at the Microwave department of TELECOM BRETAGNE, in order to allow the design and fabrication of high performance and compact microwave and millimeter wave modules, which is not possible with conventional packaging technologies. First, we briefly explain the motivations of our choice of LTCC material and compare it with other available commercial tape systems. Next, we present the manufacturing steps of LTCC and thereafter the validation of the process using available equipments at our laboratory. The manufacturing steps include tape preparation, via and cavity formation, via filling, screen printing, stacking, lamination and co-firing. We then describe, investigate and propose solutions for technological problems encountered during the validation procedure. Finally, the LTCC DESIGN RULES are defined according to the available equipments and the realized test tiles.

2.1 Choice of LTCC material

The design process of RF components begins with the selection of the best fit in terms of substrate and metalization system. The choice of suitable material is critical when packaging at microwave and millimeter wave frequencies because it affects the dimension, impedance and loss of the system. Beyond electrical, mechanical and thermal properties of substrate materials discussed in section 1.3, another important criteria for substrate selection that will be discussed in this section is the maximum operating frequency limitations. In addition, a key consideration that must be taken into account when choosing a new substrate material is the geometrical parameters of the designed transmission lines, which are very important for the manufacturing process.

2.1.1 Maximum operating frequency limitations

The maximum operating frequency limitations normally depend on the excited higher order modes. For example, in a microstrip line, different types of higher-order modes such as microstrip dielectric modes can exist and several maximum operating frequencies are defined. These frequencies are strongly dependent on the dielectric constant, substrate thickness and in some cases strip width. A detailed study is reported in [1, 2, 3].

2.1.1.1 Microstrip dielectric mode

Microstrip dielectric mode or substrate mode can be excited in a dielectric slab backed by a ground plane which supports a TM mode at high frequencies. The problem starts when the TM mode in the dielectric substrate couples to the quasi-TEM mode of the microstrip line.

The upper limit of the cut-off frequency of the exited TM mode is given by Equation 2.1:

$$f_{c1} = \frac{c \arctan(\varepsilon_r)}{\sqrt{2\varepsilon_r - 1}\pi h} \tag{2.1}$$

where c is the free-space velocity, h is the substrate height and ε_r is the relative permittivity.

Figure 2.1 plots f_{c1} versus substrate thickness of a microstrip line as function of several commercial LTCC tapes with different dielectric constant values. For example, the f_{c1} of HEREAUS CT2000 tape ($\varepsilon_r = 9.1$) is about 240 GHz for 150 μm tape thickness while the f_{c1} of ESL41110 tape ($\varepsilon_r = 4.2$) is about 345 GHz for the same tape thickness.

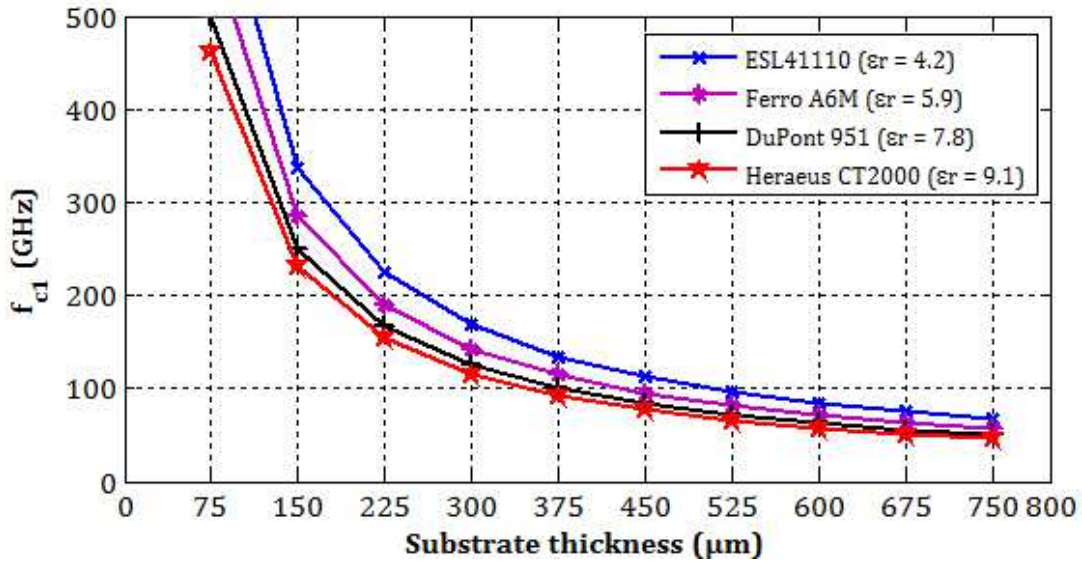


Figure 2.1: Maximum operating frequency f_{c1} of excited microstrip dielectric mode in a microstrip line for some LTCC tapes as a function of the substrate thickness

So f_{c1} is the maximum usable frequency for a microstrip line to avoid the excitation of the microstrip dielectric mode where there is no discontinuity in the transmission lines. If there is a discontinuity such as in the case of two microstrip lines with different widths, a second critical frequency called f_{c2} is defined by Equation 2.2 [3] for the excited substrate TM mode:

$$f_{c2} = \frac{c}{\sqrt{\varepsilon_r} 4h} \tag{2.2}$$

where c is the free-space velocity, h is the substrate height and ε_r is the relative permittivity.

Similarly, as represented in Figure 2.2, the maximum frequency of the excited microstrip mode for the ESL41110 material is greater than the other substrate materials due to its low relative permittivity.

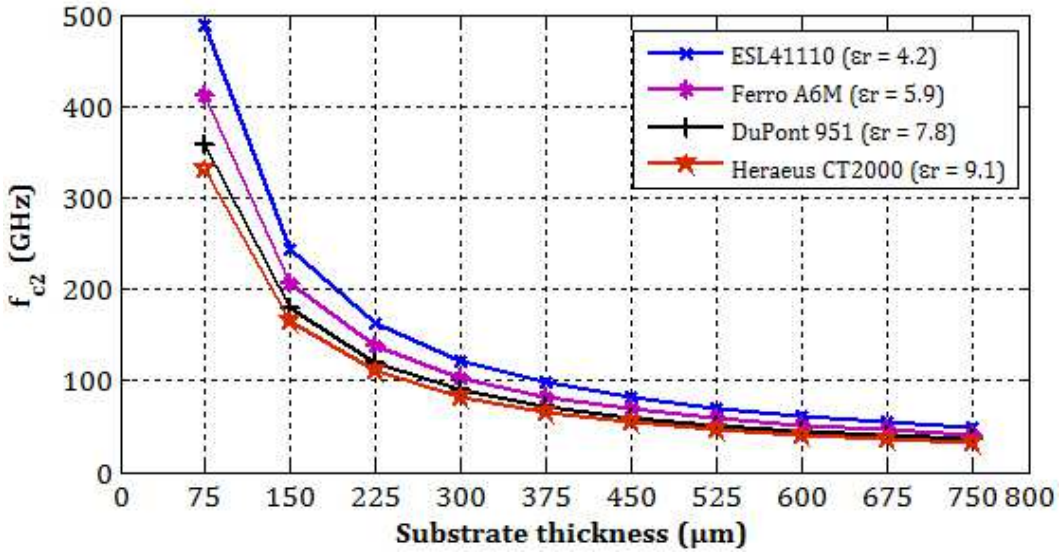


Figure 2.2: Maximum frequency f_{c2} of excited dielectric mode in a microstrip line with discontinuity for some LTCC tapes as a function of the substrate thickness

Therefore in order to avoid higher-order dielectric mode, the substrate thickness must not exceed 525 μm for operating frequency up to 60 GHz.

2.1.1.2 Higher-order microstrip mode

In the same way, in a wide strip, the most of electromagnetic energy is concentrated between the strip and the ground plane with approximate magnetic walls on the side of the strip. Therefore, as the frequency increases, a new mode generally called higher-order microstrip mode, which is similar to the parallel-plate waveguide mode (Transverse-Electric (TE) parallel plate mode) can be excited. The frequency of the first higher-order microstrip mode is defined in Equation 2.3 [2]:

$$f_{TE1} = \frac{c}{4 \cdot h \cdot \sqrt{2\varepsilon_r - 1}} \tag{2.3}$$

where c is the free-space velocity, h is the substrate height and ε_r is the relative permittivity.

The next curves plotted on Figure 2.3 represent the cut-off frequency of the first higher-order microstrip mode (TE_1) as a function of the substrate height (h) for different values of relative permittivity. The ESL41110 ($\varepsilon_r = 4.2$) substrate shows a cut-off frequency at about 100 GHz for 300 μm substrate thickness, while the cut-off frequency of the HERAEUS CT2000 ($\varepsilon_r = 9.1$) substrate for the same thickness is about 60 GHz. Thus, it is necessary to take this into consideration especially in the case of millimeter wave frequency applications.

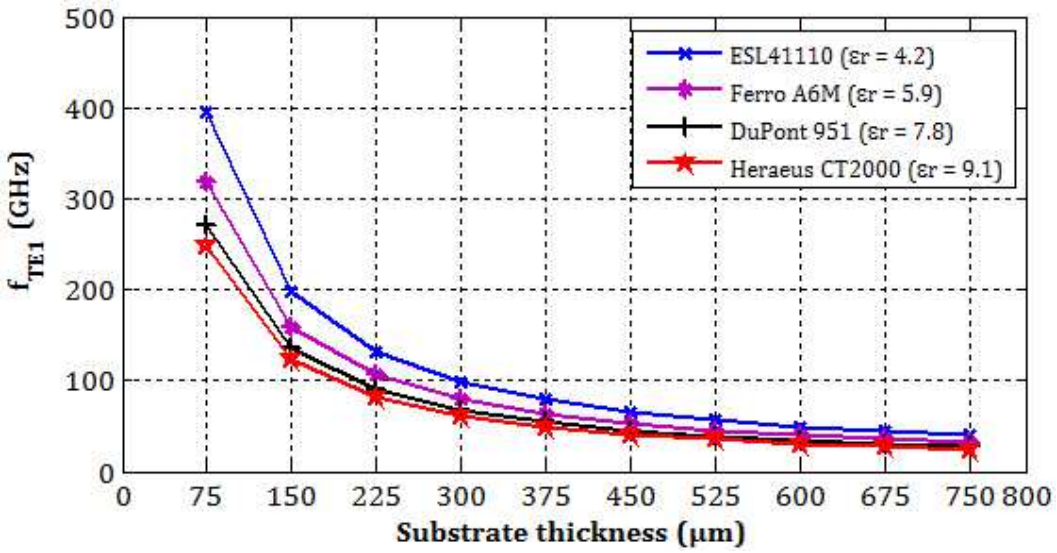


Figure 2.3: Cut-off frequency TE_1 of some commercial LTCC tapes as a function of the substrate thickness

2.1.1.3 Transverse microstrip resonance

The transverse microstrip resonance mode occurs in wide strip when electromagnetic energy bounces between the edges of the strip with the discontinuity at the strip edges forming a weak boundary. The transmission line become a half wavelength resonant structure with cut-off frequency given by Equation 2.4 [2]

$$f_{CT1} = \frac{c}{\sqrt{\varepsilon_r}(2w + 0.8h)} \tag{2.4}$$

where w is the strip width, h is the substrate height and ε_r is the relative permittivity.

Table 2.1 shows the cut-off frequency f_{CT1} of the excited mode in a 50 Ω microstrip line as function of the substrate height for some LTCC materials. The f_{CT1} decreases as the substrate thickness and the relative permittivity increase.

In conclusion, to avoid surface wave modes, for example in a microstrip line, f_{c1}, f_{c2}, f_{TE1} and f_{CT1} should be kept well above the operating frequencies. Then, the relative permittivity as well as the layer thickness should be chosen as small as possible.

2.1.2 Manufacturing process consideration

In order to avoid difficulties in the screen printing process, an important consideration is to select a substrate material with low relative permittivity, which entails wide printed lines. Table 2.1 shows the width of a 50 Ω microstrip line calculated by LineCalc integrated in

Table 2.1: Cut-off frequency of the lowest order transverse resonance mode of 50 Ω microstrip line for some commercial LTCC tapes

LTCC Tape	Relative permittivity (ε_r)	Substrate height h (μm)	Microstrip width $w_{50\,\Omega}$ (μm)	Frequency f_{CT1} (GHz)
ESL41110	4.2	75	140	430
		300	580	104.6
		600	1180	51.5
Ferro A6M	5.9	75	105	457
		300	445	109
		600	908	53.8
Dupont 951	7.8	75	81	483
		300	350	114
		600	716	56
Heraeus CT2000	9.1	75	70	497
		300	302	117
		600	622	57.7

ADVANCED DESIGN SYSTEM (ADS®) [4] for some commercial LTCC tapes according to the substrate thickness. The ESL41110 tape with relative permittivity of 4.2 allows the largest microstrip line relative to the other LTCC tapes. The microstrip width on one fired LTCC layer ($h = 75\ \mu m$) is about 140 μm, which can simply be achieved using screen printing process.

Finally, and taking into account the criteria given above, we have chosen the materials from the American manufacturer ESL for our development. Table 2.2 lists the various materials selected to install this technology. These materials include, in addition to the low relative permittivity tape ESL41110, the ESL41060 dielectric tape with high relative permettivity ($\varepsilon_r = 18$) necessary to create capacitive elements. The paste conductors are the ESL802 for via fill and ESL803 for conductor pattern. The gold-platinum conductor (5873-G) is used for SMD soldering, and the fugitive ESL49000 material is required for cavity filling during the lamination step. The full characteristics of these materials are found in Appendix B

Table 2.2: Selected materials for LTCC technology development

Material	Type	Properties
ESL41110	Low relative permittivity substrate	$\varepsilon_r = 4.2$
ESL41060	High relative permittivity substrate	$\varepsilon_r = 18$
ESL802	Via fill gold conductor	$\rho = 22.8\ m\Omega/\square$
ESL803	Pattern gold conductor	$\rho = 5.9\ m\Omega/\square$
5873-G	Gold-Platinum conductor	$\rho = 46.5\ m\Omega/\square$
ESl49000	Cavity fill fugitive material	–

2.2 Design and Layout

The design of LTCC circuits is as challenging as some cases of hybrid and thick film circuits, with increased complexity according to the layer count (up to 50 layers) and the field of application. Generally, the design process of LTCC circuits will be started with a clearly defined idea or concept. Then, with the help of Computer Aided Design (CAD) software, schematic circuit drawing, Electro-Magnetic (EM) modeling and layout processing, the solution is optimized in order to obtain an accurate design and fabrication process. As shown in Figure 2.4, the CAD design process of LTCC circuits is divided into two parts. The first that will be discussed in the next chapter (section 3.2) is dedicated to the design aspects of circuits in terms of electrical and electromagnetic parameters. The second part, which is our main interest in this section refers to the layout processing that is needed for the manufacturing process validation.

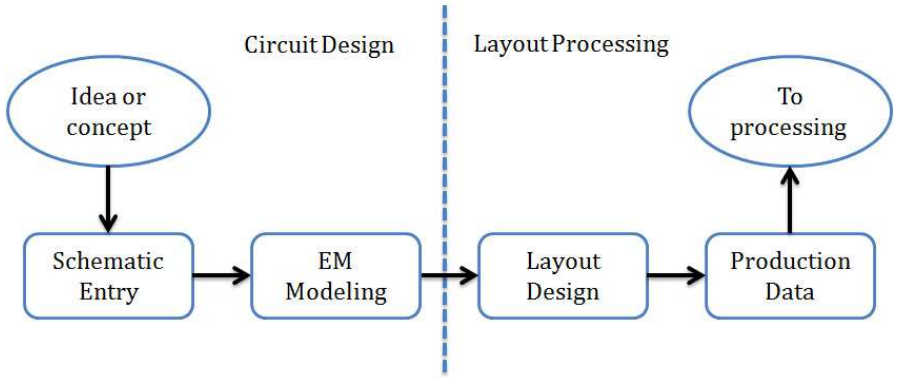


Figure 2.4: Design process of LTCC circuits using CAD software

2.2.1 Software requirements for LTCC design

Usually, simple LTCC layouts can be processed using PCB design softwares such as SPRINT-LAYOUT® [5] or ALTIUM DESIGNER® [6]. These softwares allow drawing the tape borders, cavities and the layout verification by Design Rule Check (DRC)[7], but they lack some characteristics needed for designing specific and complex LTCC modules. We summarize below CAD software requirements for complex LTCC circuits:

- Electrical schematic design
- Control of $x-y$ shrinkage
- Support multilayer substrate for screen printing and via formation
- Import/Export drawings in DXF, DRILL-MILL, HPGL and GERBER formats
- 3D structure visualization

In our laboratory, we use ADS® from AGILENT TECHNOLOGIES to design and prototype our LTCC circuits. ADS® software responds to the most criteria cited above and it allows us to output the necessary file formats required for the fabrication process. These files include HPGL for creating the screen printing and via fill masks by the photo plotters while DXF and DRL files are used for both LTCC tape cut and via formation by laser. A problem appears in the exported DRL files when using it with our laser machine. In order to resolve this problem, we re-import these DRL files into GERBTOOL® [8] software and export it again to get the correct DRL files.

Figure 2.5 illustrates the layout processing before manufacturing steps. In order to start our manufacturing process and create our own DESIGN RULES, we based our early work on standard LTCC DESIGN RULES available from the other LTCC manufacturers.

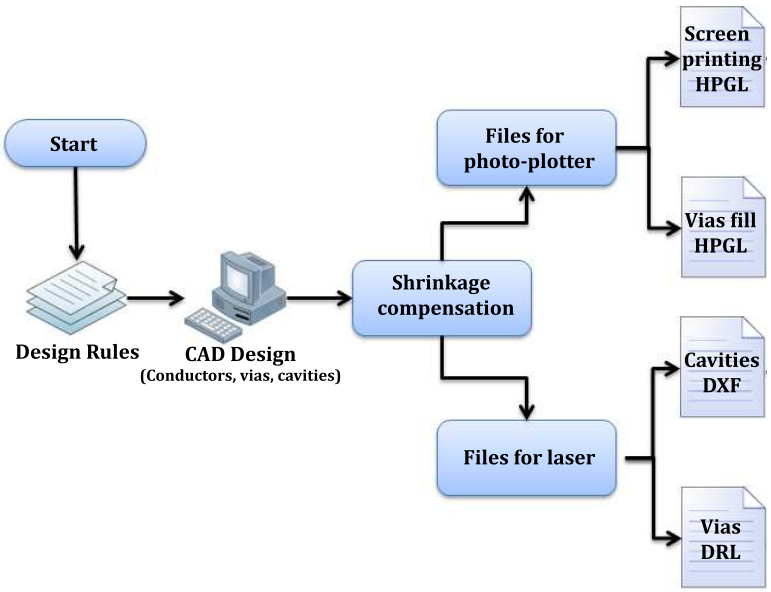


Figure 2.5: Layout processing of LTCC circuits

2.3 LTCC process

As discussed in section 1.2.3, the ceramic-glass powder and organic binder are mixed to make a slurry. The slurry is tape-casted using doctor blade resulting in a LTCC sheet (GREEN TAPE®). After selecting the required materials for our applications, it is necessary to validate the manufacturing process of LTCC circuits. Manufacturing of LTCC multilayer circuits is a multi-step process, which is easy to understand, and complex to realize due to that several parameters vary upon the equipments employed.

The purpose of this section is to give a general overview on LTCC process flow required to manufacture LTCC circuits combined with the development of this process using our equipments. Figure 2.6 shows a simplified process flow for a typical LTCC build.

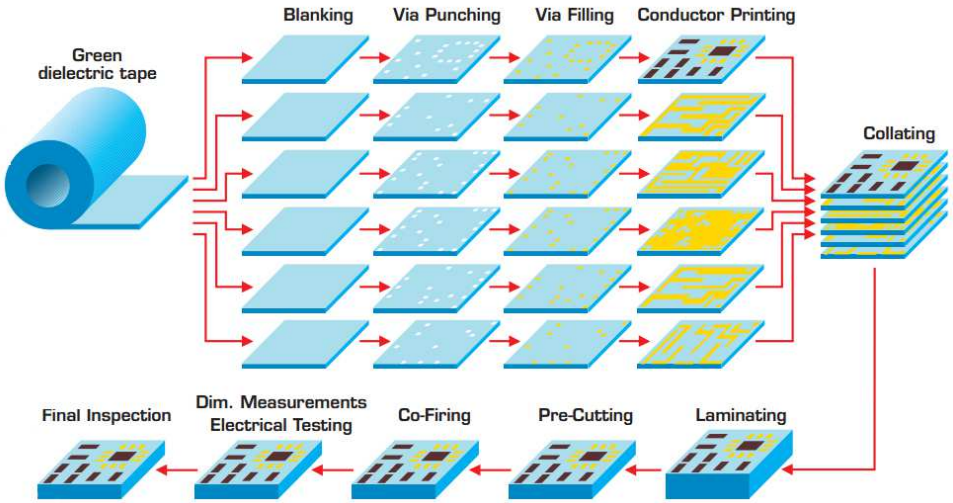


Figure 2.6: LTCC process flow (Source: DT-MICROCIRCUIT [9])

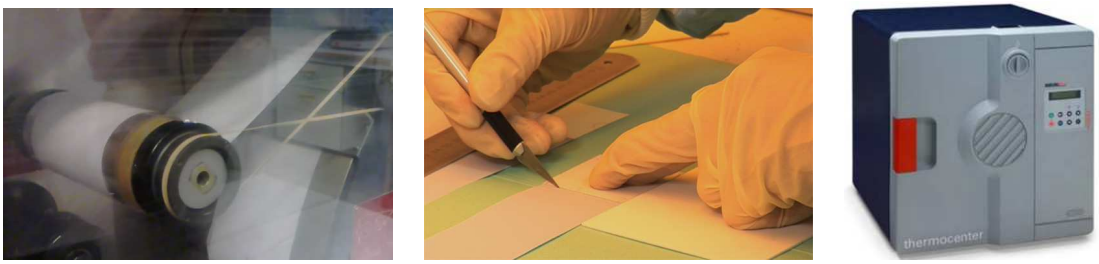
2.3.1 Tape preparation

2.3.1.1 Slitting and blanking

Often, the LTCC green tapes are shipped on a roll. The rolled tape needs to be cut to specified widths along the length of the coil. This process is known as slitting. Next, the coils are blanked, this mean that the LTCC layers are cut at the exact desired dimensions, in a square or rectangular forms. Standard substrate sizes are for instance $3.5'' \times 3.5''$, $3'' \times 3''$ and $2'' \times 2''$ [10], but any size can be used. Depending on the dimensions of the pin alignment fixture, this last size is chosen to cut our tapes. Normally, the sheet is cut with a razor blade, laser or a cutter system. If a laser is used, it is necessary to control the power to avoid damaging the LTCC sheet. After the cutting process, it is preferred to create an orientation mark for the printing and stacking steps. This mark serves to turn layers 90° during stacking, to compensate the $x-y$ shrinking of the LTCC. With the help of a laser or punching system, the registration holes are readily added after blanking. Finally, it is necessary to remove MYLAR® (commercial name by DUPONT® for the polyester backing tape) before the preconditioning to allow tape relaxation.

2.3.1.2 Preconditioning

Preconditioning is useful to eliminate the stress induced by the removal of the backing tape. It consists in heating LTCC tapes for stabilization in an oven for a short time. Depending on the material composition, the temperature is between $80°C$ and $120°C$, and the duration is between 15 and 30 minutes. To verify the influence of this step on the ESL41110 tapes, several tests were realized using the oven shown in Figure 2.7-(c). As a result, the lack of the preconditioning on LTCC sheets affects the final dimensions of our fired LTCC circuit and change the shrinkage value of the circuit in x, y and z directions (see section 2.4.3). Finally, according to the realized tests, the ESL41110 tapes must be heated at $80°C$ for 30 minutes.



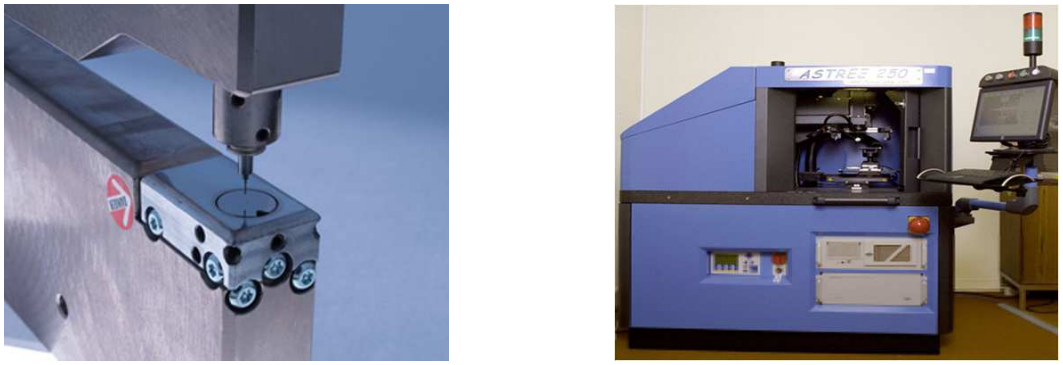
(a) (b) (c)

Figure 2.7: LTCC tape preparation: (a) Rolled LTCC tape (Source: SWEREA IVF). (b) Blanking of LTCC coils by a razor blade. (c) Oven used for LTCC tape stabilization

2.3.2 Via and cavity formation

Once each of the tape layers is prepared, the next step is normally via and cavity formation. In this process, holes are created on each layer for electrical connections between layers in the vertical axis of the substrate. Thermal vias may also be created for heat dissipation of amplifiers or other power systems. In addition, cavities and channels are cut. Channels are used for micro fluidic sensor applications. For RF applications, open cavities are traditionally used to place semiconductor chips into substrate layers to improve electrical performance by minimizing wire bond length, while the embedded air cavities are used to achieve a wide band response of stacked patch antennas and resonating structures. Normally, vias and 2D shapes are cut using two available methods: mechanical punching and laser cutting.

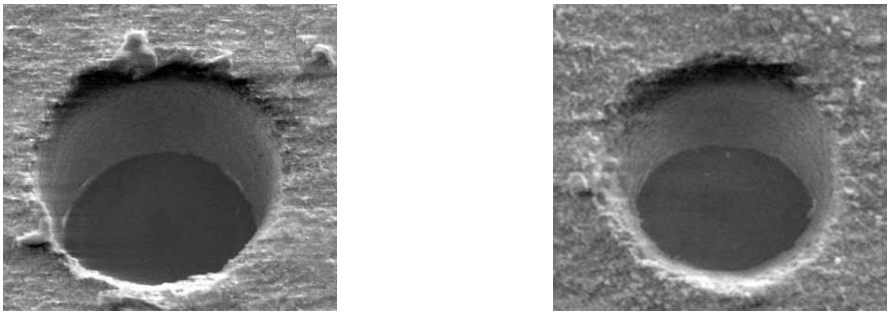
Mechanical punching is a process to create high quality vias using high speed Computer Numerical Control (CNC) mechanical punching systems (Figure 2.8-(a)). The puncher system uses the same basic principles as a paper hole punch. A punch tool is located above the desired hole location, a corresponding die is located below the desired location and the tape layer is moved. The undesired tape is cut and removed by the punching system. The vias punched are cleaner than the laser drilled vias, and form an ideal cylindrical form along the tape thickness.



(a) (b)

Figure 2.8: Via and cavity formation tools: (a) Mechanical puncher system (source IMST). (b) Our Nd-YAG laser system

Laser drilling may also be used with as the CO_2 or Neodymium-doped Yttrium Aluminum Garnet (ND-YAG) laser system that is used for cutting our LTCC tapes. The quality of the drilled holes will not be as good as one being punched mechanically. Figure 2.9 compares the measured data for 100 μm via diameter for mechanically punched (Figure 2.9-(a)) and laser drilled (Figure 2.9-(b)) LTCC via. Due to their focus, the via diameter decrease - in the case of laser drilling - more than 20 % on the opposite side of LTCC tape [11]. The advantage of lasers, that are the most popular for channel and cavity formation, is its ability to cut complex shapes with rounded or curved edges. Another benefit of laser systems over the mechanical punchers is that there is no need to change the drilling tools for each different via diameter.



(a) (b)

Figure 2.9: Mechanical punching (a) vs. Laser cut (b) of 100 μm via on LTCC sheet [11]

Our laser machine is a ASTREE 250 model (Figure 2.8 -(b)) from NOVALSE society. This laser is dedicated to the micro-cutting and micro-drilling of different composites and materials such as ceramic, plastic and metal. This laser is indeed a ND-YAG source with wavelength of 1064 nm and frequency between 20 and 100 kHz. The maximal output power is 16 W (at 100 kHz) and the spot size is around 50 μm. In order to achieve small and clean vias, we made a range of experiments on our LTCC tapes taken into account the thickness of the substrate. In practice, several parameters such as the cutting speed, the pulse repetition frequency and the output power were optimized. After optimization of the parameters, 150 μm vias were successfully drilled in the 106 μm thick ESL41110 substrate. Similarly, cavities and other shapes are easily performed. Figure 2.10 shows 224 vias which are machined in our ESL41110 tape. The laser is configured for 5 W output power. The pulse repetition rate was fixed at 80 kHz and the cutting speed is 10 mm/s. As the figure implies, the obtained via diameter is at about 200 μm, with a tolerance of $\pm$ 25 μm related to our laser system.

2.3.3 Via fill

After via creation in individual layers, the next important technological step is via fill process. Via holes must be filled with a thick film conductor to ensure electrical connection between layers. This process is generally completed with the help of conventional stencil/screen printer system. The stencil process is very similar to the thick film screen printing method. In the case of a via diameter less than 150 μm, to obtain high quality filled vias, it is necessary to use

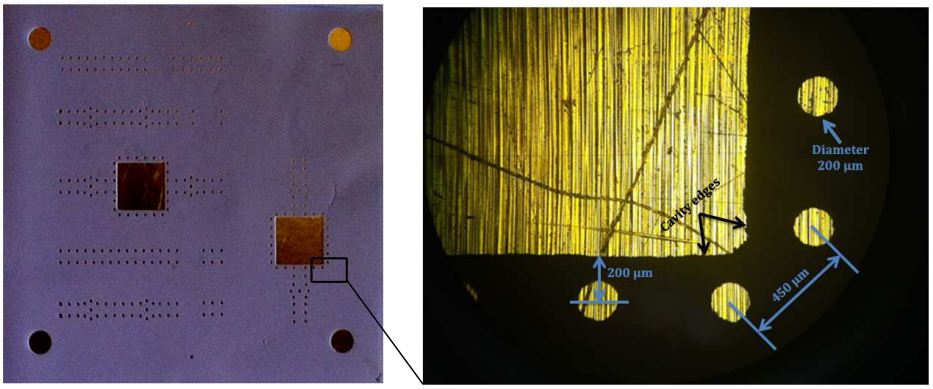


Figure 2.10: 224 drilled vias of a 106 μm ESL41110 tape using ND-YAG laser system. The via diameter is 200 μm, the via pitch is 450 μm and the via to cavity edge distance is 200 μm

metal stencil instead of a mesh screen, because the ink injected in the holes can be blocked by the mesh which results in poorly filled holes.

Figure 2.11 shows the process of stencil printing. The stencil is generally laser cut or chemically etched with identical vias to those on LTCC layer. The LTCC sheet is placed on a porous stone that ensures the optimal distribution of vacuum to hold the tape in place during the filling process. An absorbent paper must be placed under dielectric sheet to avoid via paste get across the porous stone. To accomplish a proper fill, the ink viscosity, process setting and mask to substrate alignment must be adjusted. An accurate alignment can be achieved with an optical positioning system. Once tape, ink and machine setup have been prepared, paste is applied through the stencil apertures above via holes and it is absorbed with a vacuum pump into the holes to fill them. Finally, according to the used paste, the filled vias are dried in a oven between 5 and 15 minutes at a temperature between 80°C and 120°C.

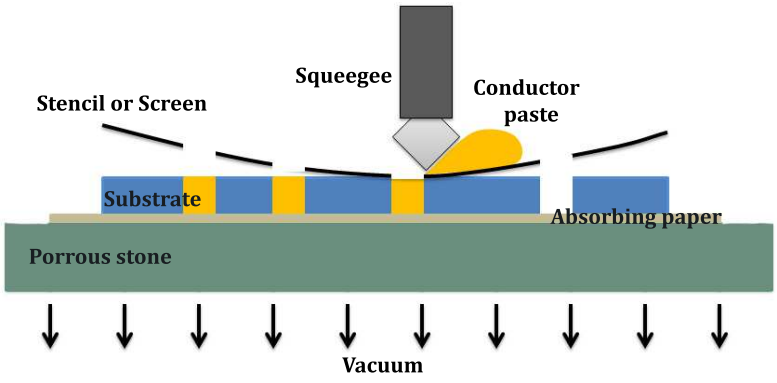
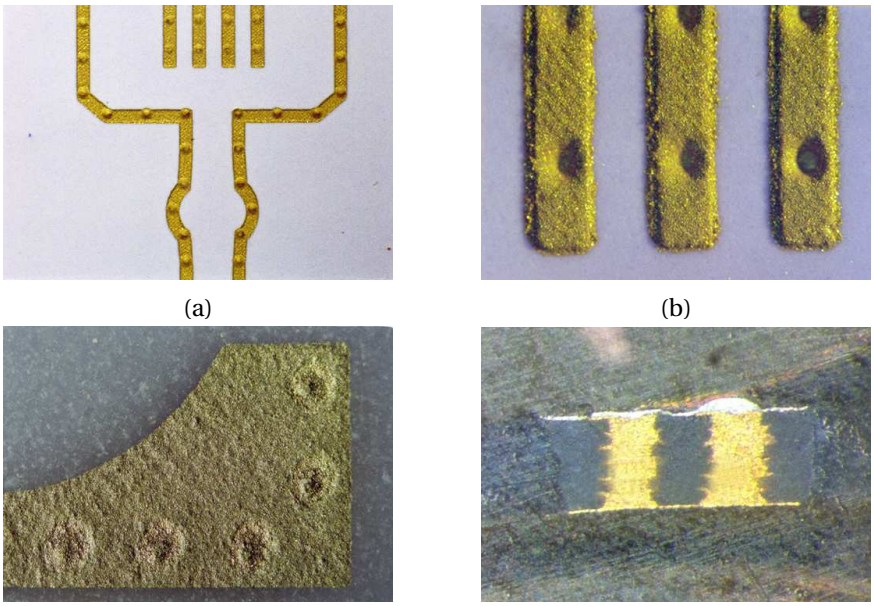


Figure 2.11: Filling via holes of LTCC sheets with stencil/screen printing technique

The via fill process of our LTCC tapes is performed with the semi-automated thick film screen printer model CP-465 from PRESCO. The specific gold paste ESL802 is used to fill our drilled LTCC vias through a 325 mesh screen. Knowing that there are some difficulties with the

meshed screen, we it took several tests and screen printer configurations to finally manage to fill the vias properly. We also note that the vias filled with ESL802 paste are dried at 120°C during 10 minutes. Figure 2.12 shows successfully filled vias by ESL802 paste using a 325 mesh screen. The figures (a) and (b) illustrate filled vias with diameter of 225 μm on unfired ESL41110 tape, while (c) and (d) show filled vias after firing of six ESL41110 layers. The via diameter on the fired LTCC is 180 μm and the spacing (center to center) is about 450 μm.



(a) (b)

(c) (d)

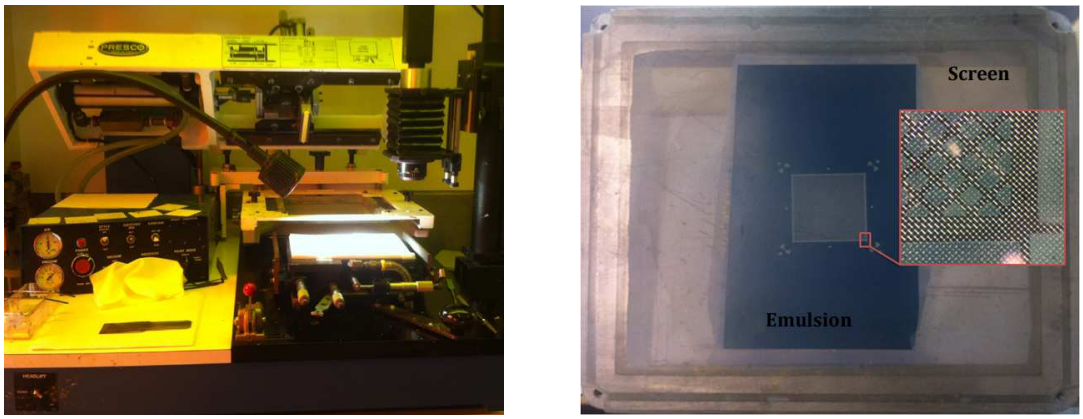
Figure 2.12: Some filled vias before (top) and after (bottom) firing of LTCC layers

2.3.4 Screen printing

Once all vias have been formed and filled to create vertical interconnects between layers, the horizontal interconnects are next patterned across the surface of each layer. As on hybrid thick film circuits, the patterns on LTCC are implemented by screen printing method. The main drawback of this method is limited by the screen openings and only line widths and spaces down to 100 μm can be achieved. In addition, the tolerances are important due to the mesh on the screen which translates to electrical tolerances, especially at millimeter wave frequencies. For this reason, a new technique called PHOTO-IMAGED® pattern on LTCC, was developed by DUPONT®, it consists in combining thick film and photo-lithography materials, in order to obtain very fine printing lines (width down to 20 μm) on LTCC substrate with low fabrication tolerances.

The screen printing process has the same basis as stencil printing described above (see Figure 2.11), but a difference is that the stencil is a sheet of stainless steel, whereas the screen is a stainless steel mesh. A meshed screen is generally composed of weaved fine wires that are mounted on a metallic frame like Aluminum. A photo-emulsion that is a photosensitive

polymer coating is sensitive to Ultra-Violet (UV) light is placed onto the screen. The emulsion blocks the screen mesh and allows the paste to flow only through desired openings to form a pattern on the substrate. Figure 2.13 shows the screen printer as well as a 325 meshed screen used in our screen printing operations.



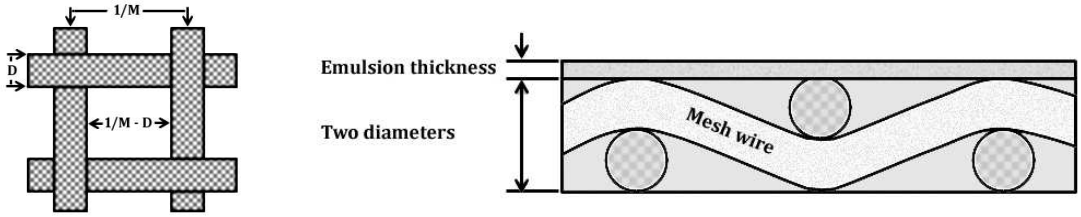
(a) (b)

Figure 2.13: Screen printing operations: (a) PRESCO CP-465 machine printer with camera for optical alignment. (b) A 325 screen mesh count of a meshed ground plane with emulsion thickness of 20 μm

The LTCC substrate offers better printing resolution than standard thick film conductors on Alumina, due to the flatness of the unfired LTCC tape. Resolution and thickness of the printed layer are influenced by the screen specifications, process setting and ink properties.

The first consideration that is necessary to take into account when using screen printing technique is to select the right screen to obtain a good quality pattern. A screen is usually characterized by the mesh count, wire diameter and the open area. The mesh count represent the number of wires per inch and may vary from 80 wires per inch, for coarse printing such as solder paste and resistor thick film, up to 400 wires per inch for fine line printing. Beyond the photosensitive emulsion thickness, the mesh thickness, which is approximately twice of the wire diameter, plays a more important role on the thickness of the deposited patterns. Finally, as shown in Figure 2.14-(a), the size of the opening calculated according to the mesh count (M) and the wire diameter (D), affects the amount of paste that can be transferred to the substrate during the printing process.

Another important factor which influences the quality of screen printing is the selection of the proper setting of the screen printer. This includes the printing speed, squeegee pressure, snap-off distance and squeegee angle. The most important parameter is the printing speed, which can be adjusted according to the paste viscosity. If the squeegee speed is too fast, this can resulting in a thinner print than normal, due to the insufficient paste transferred to the substrate. In contrast, if the speed is too slow, the paste may not be properly sheared, and the print may be too thick. The squeegee pressure depends on the snap-off distance (screen to substrate distance). High squeegee pressure is needed in the case of a high viscous paste because, if the pressure is not sufficient, this may result in a thick print with poor definition.



(a) (b)

Figure 2.14: A meshed screen characteristic: (a) Cross section of screen and emulsion. (b)Screen opening

The paste is a mixture of a metal powder, glass and adhesion elements. Thick film paste properties include viscosity, particle size and solid contents. Only, the viscosity can be increased by the use of thinner solvents. Finally, depending on the paste features, the patterned conductors must be dried, after printing, in an oven. The temperature may vary between 80 and 120°C during 5 to 15 minutes.

After the presentation of screen printing method, another technique is also used today for conductor patterning on LTCC substrate: the so called FODEL PHOTO-IMAGEABLE® technique that was developed by DUPONT® to achieve precise and narrow (several tens of microns) printed patterns on adapted LTCC sheets. This technique, which combines thick film materials and photo-lithography [12], is only possible on inside layers for the DUPONT 951 LTCC tapes. For others, such as FERRO A6-S, only external surfaces are photo-imaged.

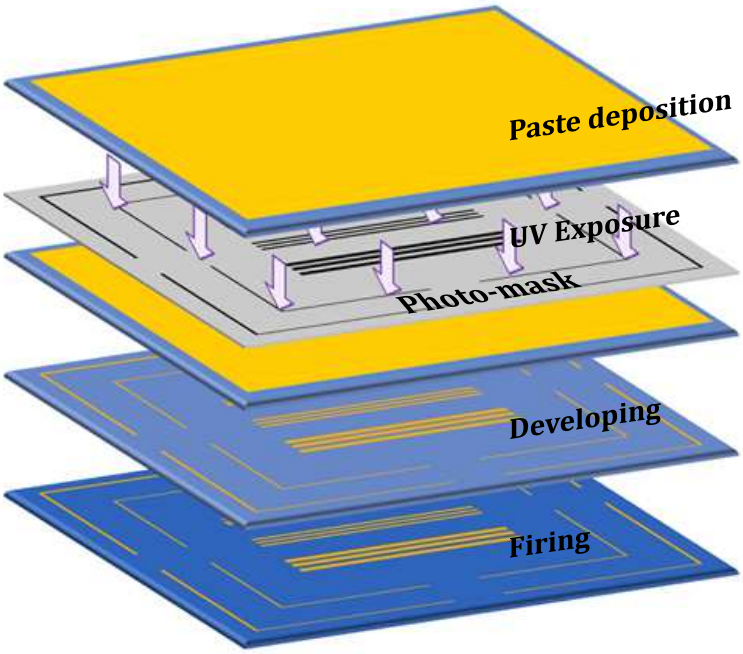
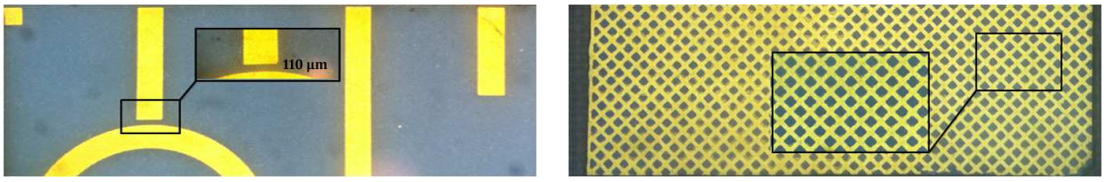


Figure 2.15: Photoimageable process flow

The process flow of fabrication of photo-imaged patterns is shown in Figure 2.15. Using standard thick film printer, a special conductor paste is deposited across the LTCC sheet. The printed ink is dried and next the layer is exposed to UV light through a photo-mask containing the desired pattern. Using a 1 % Na_2CO_3 solution, the areas that are not exposed to UV radiation are removed. The last technological step is firing in the furnace [13]. The great advantage of this technique, when compared to thin film and etching technologies is that FODEL® is the only method to obtain a higher wiring density on internal layers of LTCC substrates, whereas thin film can be applied only on fired substrates, which limits their use on outer structures.

Our screen printing operations on LTCC substrate are implemented using the same screen printer PRESCO CP-465 (Figure 2.13-(a)) used for via fill process. Screen with 325 and 400 mesh count are used to obtain fine printing resolutions. The photosensitive emulsion with 20 μm of thickness is also used for fine conductor patterns.

To validate the screen printing process, several printing tests were performed on the ESL41110 tapes with the ESL803 gold paste. The results were not encouraging and we believed that the problem was due to the paste itself. Therefore using TANAKA thick film paste [14], we obtained a high quality pattern definition. Figure 2.16-(a) shows a printed conductor line of RF structures using TANAKA paste, the gap between the microstrip line and the ring is about 110 μm. But the main problem of TANAKA paste is that it is not compatible with LTCC tapes in term of shrinkage. All these problems are extensively explained in section 2.4.1. Finally, by re-using of the ESL803 paste, and after several tests, a successfully pattern with width and space down to 120 $\pm\,\mu m$ are achieved. As represented on the Figure 2.16-(b), the meshed ground plane is implemented on ESL41110 tape with the ESL803 paste. The conductor width and space are 200 μm and 400 μm respectively, and the shrinkage value of the LTCC substrate is in the range. The ESL803 paste is thus used for conductor patterning on ESL41110 LTCC substrate.



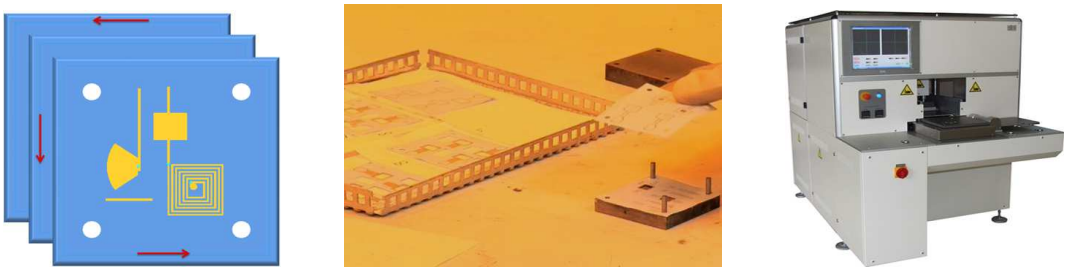
(a) (b)

Figure 2.16: A successful conductor pattern on ESL41110 using screen printing technique: (a) Example of printed conductor lines with the TANAKA thick film paste, the conductor width is 700 μm and the gap between the microstrip line and the ring is at about 110 μm. (b) A meshed ground plane patterned with the ESL803 paste, the conductor width is 200 μm and the space between two conductor is 400 μm

2.3.5 Stacking and alignment

The purpose of the aligning process is to make a three dimensional multilayer structure from blanked, via filled and screen printed LTCC sheets. The principle of this step is to stack - using an aligner - layer by layer in the proper order from layer 1 to layer n. The adjacent sheets should be 90° rotated as shown in Figure 2.17-(a), because the shrinkage in the $x-y$ direction may be different from one layer to another due to the tape casting process. This rotation is taken into account by marking the LTCC layers during the tape preparation process (section 2.3.1). The two key requirements in this process are precise layer to layer alignment and strong bonding between layers.

Today, there are two available methods for alignment process, manual by using pin alignment fixtures or automatic alignment with vision system. The pin alignment fixtures are fabricated of stainless steel and have generally four pins located at the corners of the fixture. The individual layers provided with the registration holes are slipped over the pin and then down on the metal plate. The drawback of this method is that the tape layers tend to stretch and the registration holes in the tape are deformed by the pins. As a result, it is very difficult to obtain an alignment error less than 50 μm using this method. Another approach, offering a high alignment accuracy, is to use an automatic stacking machine based on camera systems and computer based machine visions (Figure 2.17-(c)). With this method, alignment errors can be minimized to 10 μm.



(a) (b) (c)

Figure 2.17: LTCC stacking and alignment: (a) Rotation of LTCC layers during stacking for shrinkage compensation. (b) The pin alignment fixture used in our laboratory for manually stacking operations. (c) An automatic stacker machine with optical vision system

Our LTCC layers are stacked with the help of the pin alignment fixture represented in the Figure 2.17-(b). This fixture is composed of three pins instead of four pins, to minimize the stretching of the layers during stacking. A protecting material is used at the start and the end of stacking operation to avoid the contact of LTCC material with the metal plates during lamination. Finally, in order to obtain better bonding between the stacked layers as well as the protective materials, we place it, after sealing the LTCC sheet corners, under vacuum to evacuate the air located between the LTCC layers (Figure 2.18).

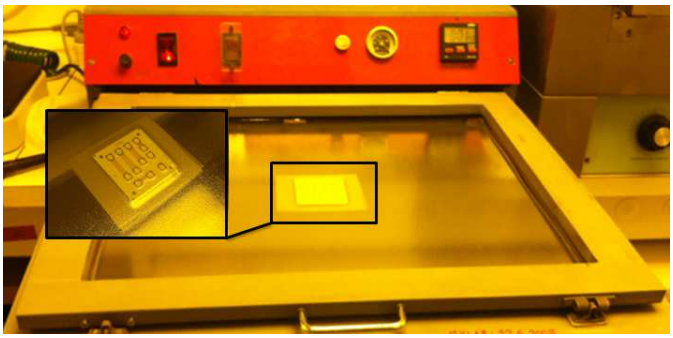
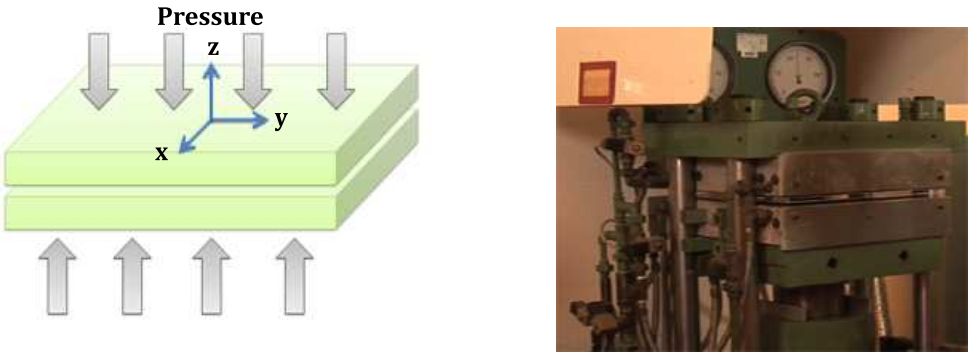


Figure 2.18: Placing of stacked LTCC layers under vacuum for air voiding located between layers

2.3.6 Lamination

Once the layers are stacked, the green sheets are laminated under heat and pressure to ensure a strong contact between layers and to avoid delamination. Pressure, high temperature and time can be varied from one LTCC manufacturer to another, because it is related to the green tape properties. Generally, common process conditions are 200 $bars$, 70°C for 10 minutes. The high pressure and elevated temperature enable good adhesion between adjacent layers. After lamination the structure is ready for firing in a furnace. Normally, there are two available methods to laminate the stacked layers: the uniaxial and isostatic method.

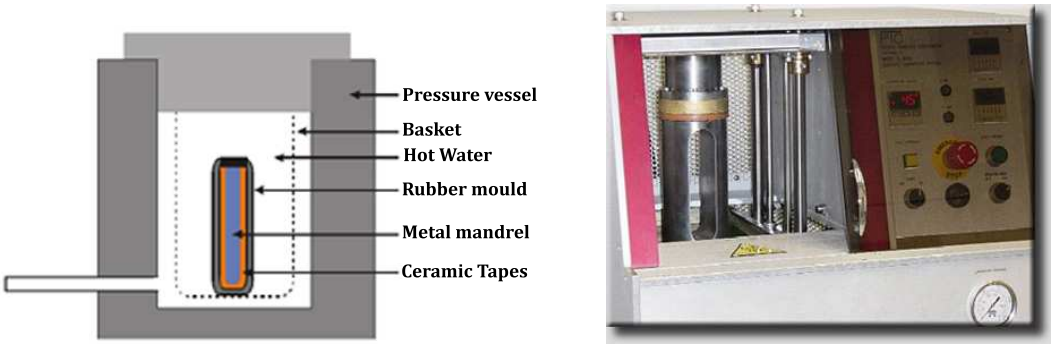
The first method is achieved with the use of a uniaxial press machine as represented in Figure 2.19. The principle of uniaxial pressing is to place the stacked LTCC layers between two heated plates and press them selecting the recommended process parameters. This method is characterized by speed and simplicity. The uniaxial lamination could cause difficulties in establishing perfect parallel lamination, and can create variability in the pressure and temperature. In this case, the substrate density is strongly affected, which then results in high shrinkage variations during firing (see section 2.4.3), and in thickness variations. In addition, this approach can also cause deformation of cavity structures.



(a) (b)

Figure 2.19: Lamination with uniaxial method: (a) Uniaxial pressing principle. (b) Uniaxial press machine used in our laboratory

The second method uses an isostatic press. The LTCC substrate is pressed in hot water at about 350 $bars$. The temperature and time remain unchanged. The isostatic method is more complex than uniaxial technique because the contact between the unfired module and water should be avoided. For this reason, the stacked tapes are vacuum packaged in a foil to prevent introduction of water into the substrate. Figure 2.20 shows the principle of isostatic press lamination.



(a) (b)

Figure 2.20: Lamination with isostatic method: (a) Isostatic pressing principle. (b) Isostatic press machine Model IL-4004 used at IMST [10]

Our stacked green tapes are uniaxially laminated with the machine illustrated in Figure 2.19-(b). At the start of our first lamination tests, we pressed the LTCC layers placed in the pin alignment fixture. This result in an important mechanical distortion of the laminated circuit (see section 2.4.2) due to the lack of the fourth pin in the fixture. A new technique developed at the laboratory consists in lamination of the stack LTCC layers without the aligner tool. The LTCC layers are sealed at the corners after stacking process and next placed after air voiding between two stainless plates. Finally, the LTCC layers are laminated at 200 $bars$, 70°C for 10 minutes. ESL49000 fugitive inserts are used inside the cavities to avoid geometry deformation during the lamination process. Figure 2.21 shows a laminated LTCC circuit composed of eight layers. The ESL49000 inserts placed in the cavities during stacking are also bonded to LTCC materials. After lamination, the pressed substrate is pre-cut to half of the substrate thickness using a heated blade, meeting the circuit drawing specification.

2.3.7 Co-firing

Once the green sheets are stacked and pressed, the laminated structures are fired using a specific firing profile to obtain a mono-bloc circuit. As shown in Figure 2.22, this process can be completed in two ways: either a box furnace or a conveyor belt furnace. During the firing cycle, the unfired LTCC substrate must be placed on a setter. For example, setters used for FERRO A6 and FERRO L8 tapes are fused quartz, Alumina or Zirconia felt setters [15]. Generally, the setter material is selected according to the firing temperature and LTCC substrate material composition. In order to avoid deformation, bumps and cambers in the fired substrate, it is

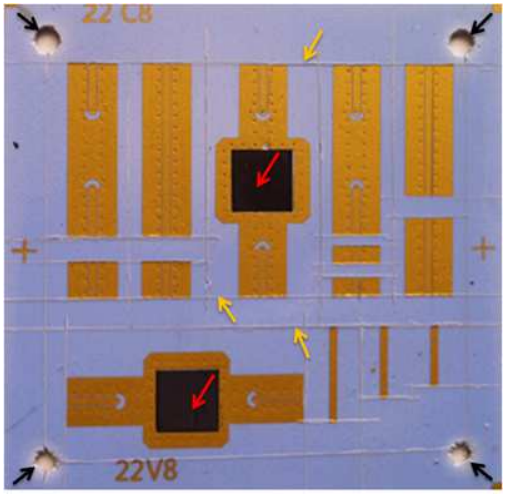
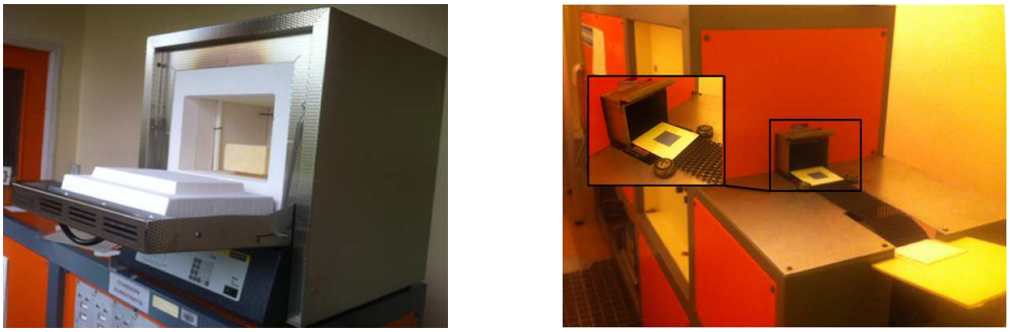


Figure 2.21: A laminated LTCC circuit using the uniaxial press machine with registration holes (black arrows), fugitive ESL49000 tape (red arrows) and manually pre-cutted circuit parts (yellow arrows)

very important to choose a very plat setter and to keep its surface very clean.

The box furnaces that can be programmed for a given temperature profile offer the possibility to have a uniform temperature distribution in the box space. This is an important feature, because the non uniform temperature across the substrate may lead to a variable shrinkage in all directions. As box furnaces are low price compared to the belt conveyor furnace, it is limited by the low volume production capability.



(a) (b)

Figure 2.22: Firing furnaces of LTCC substrate: (a) Box furnace model NABERTHERM. (b) Belt conveyor furnace, the LTCC substrate is placed on Alumina setter

The firing profile generally depends on the material composition, and must be modified in the case of large and thick substrates. The cycle time normally varies from 3 to 8 hours but, in some cases such as the new material DUPONT 9K7, it is as long as 27 hours [16]. Figure 2.23-(a) shows a typical LTCC firing profile of box furnace. The first part, intended to burn-out of the organic materials, shows a rising temperature between 350 and 450°C, followed by a one to two hour hold at that temperature. During this step, the solvents outgassed must be

removed from the furnace by ventilation. At the end of this cycle, the substrate is very fragile, and behaves as a powder, because the binders have been removed from the substrate and only the inorganic material that constitute the final substrate remains in the furnace. Once this phase is completed, the sintering stage is started and the substrate is heated to the sintering temperature that is usually between 800 and 900°C. Next, the temperature is fixed for 10 to 15 minutes, to obtain at the end of this step, the desired solid LTCC block. During sintering, the LTCC substrates shrink in x, y and z directions, this shrinkage generally varies from 10 to 20%, depending on the material composition. Figure 2.23-(c) shows the shrinkage of the substrate that affects the final circuit size of the LTCC circuit after the firing process. The last part of the LTCC firing is dedicated to the cooling cycle by reducing the firing temperature to finally return to the ambient temperature.

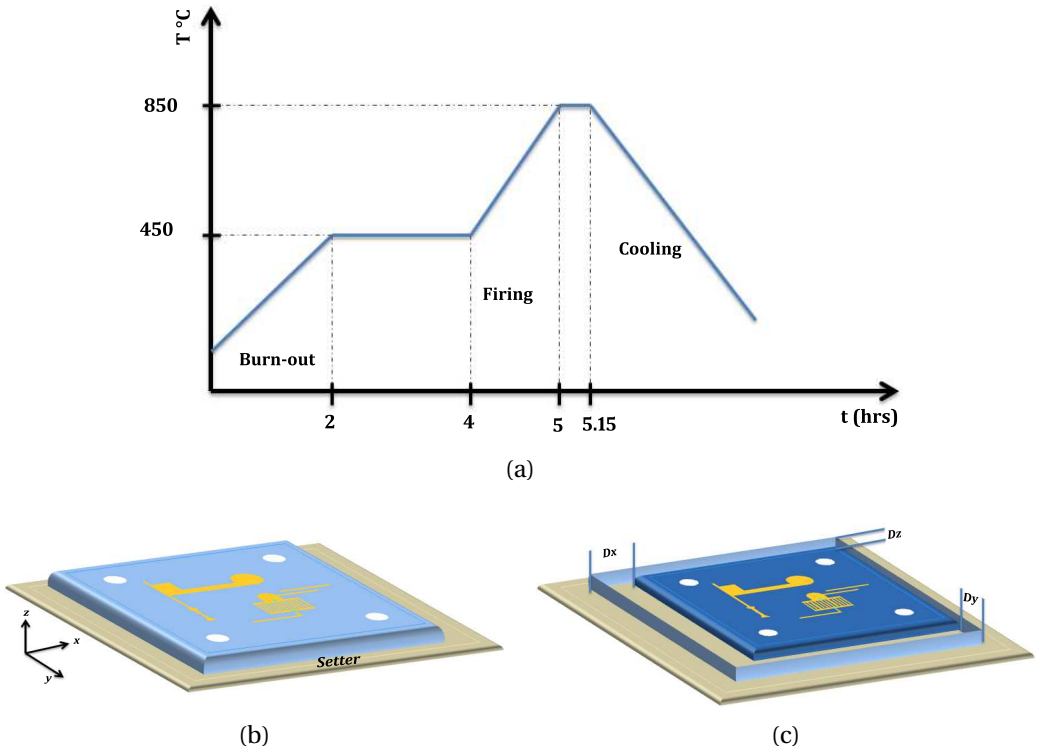
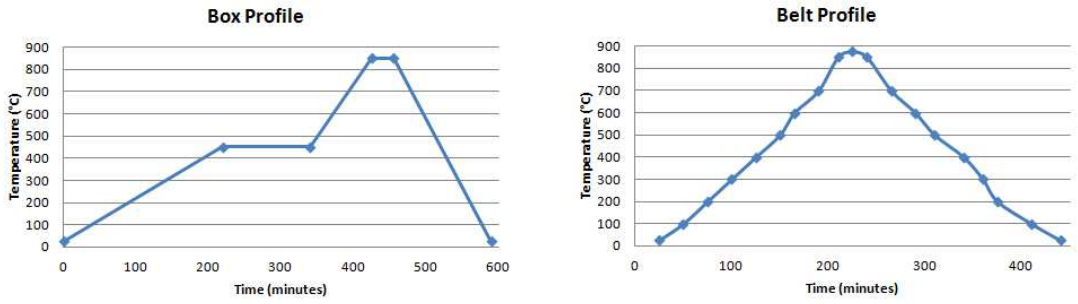


Figure 2.23: Firing of LTCC substrate: (a) A typical firing profile of LTCC materials in a box furnace. (b) LTCC circuit before firing. (c) LTCC circuit after firing

The belt furnaces are also used for burning-out and firing of LTCC substrates. Normally, a conveyor furnace is composed of multiple controlled zones which include preheating zone, binder burn out zone, heating zone, firing zone and cooling zone. These systems are generally large and their length may exceed 3 m because of the need of several zones. A belt furnace is characterized by the fast thermal response, uniform temperature distribution and continuous flow of substrates, which is very important for high volume production. Normally, the firing profile employed in the belt furnace is different than in the box furnace. Figure 2.24 shows the difference between firing profile in box and belt furnaces for the FERRO L8 tape system [15].

The hold of temperature, in the case of belt firing profile, after burn-out and firing ramps are eliminated and thus the firing cycle is reduced.



(a) (b)

Figure 2.24: Difference between box and belt firing profile for FERRO L8 LTCC material :(a) Box furnace firing profile. (b) Belt conveyor furnace profile

2.3.8 Post-processing

When the firing process is completed, the fired LTCC module is ready for the post-processing steps. This includes post-firing, singulation and final inspection.

2.3.8.1 Post-firing

Post-firing may be defined by the way to add - in some cases - metalization, resistive and dielectrical layers to the LTCC module after firing process. This means that the paste is to be applied after firing and has to be fired again. The most common post-fired pastes are gold, gold platinum and gold palladium compositions that are intended for wire bonding or brazing.

2.3.8.2 Singulation

The singulation is also an important step in which the fired modules are cut into individual circuit components. Singulation can be performed using several methods. The first used for our LTCC circuit singulation is the simplest and fastest way and consist to use a hot knife cutting system. After lamination, the unfired substrate is pre-cut in $x-y$ directions at the printed conductor edges to about the half of the substrate thickness in depth. After firing the circuit elements are broken by manual operation.

After the firing process, lasers may also be used to cut a complex shape. The tolerances are tight, but the high power produced by the laser can result in a poor quality at the edges of the cut element.

A diamond tool and dicing saw, used for semiconductor dicing, are also used to cut these type of substrates. These methods allow high quality edges.

2.3.8.3 Final inspection

This process can be performed using manual or automated inspection for reliability evaluation of fired components, failure analysis and the accordance with the applicable standards. Manual inspection includes an optical check and geometry measurement of the fired module under the microscope (Figure 2.25). Automatic inspection methods discussed in [17] use ultrasonic and X-ray scanning electron microscopes. These methods are applicable for imaging assemblies, conductor tracks and for detecting defects such as layer delamination.

Figure 2.25: 3D optical measuring microscope used in our laboratory

2.4 Technological problems

In the previous section (section 2.3), we gave a general overview of the principle and methods of prototyping LTCC circuits. In addition, we presented the implementation of this technology using the available resources in our laboratory. This technology installed thanks to this Ph.D thesis encountered several technological difficulties during validation of each step. The identification and resolution of these problems has occupied the most time in this thesis work because of the large number of parameters that affects the final prototyped circuit. We note for example, the misalignment between the layers after lamination, screen printing resolution problems, cavities deformation, bad via filling, LTCC sticking to the setter during firing, shrinkage control, etc. In this section, we present these problems in chronological way, discussing their causes and finally propose suitable solutions.

2.4.1 Screen printing problems

After receiving the necessary materials for the implementation of LTCC technology (see Table 2.2), we start our manufacturing process validation with simple circuits in order to verify the ability, as well as the limits of our equipments. The first step is to transfer our experience in screen printing on hybrid thick film substrate, such as Alumina, to LTCC substrate. The process is very similar but it is necessary to take the physical properties of LTCC tape into account, such as the substrate thickness and surface behavior.

Figure 2.26 presents the first realized LTCC circuit, which is composed of five ESL41110 layers. The top layer is screen printed by simple lines and pads in x and y direction. The width and gap of lines vary from 300 μm to 75 μm and, pads size (width and diameter) are between 1000 μm and 75 μm. To compensate the shrinkage of circuit after firing, all patterns are scaled (+ 15 %) at the design step. All layers are cut in 50.8 × 50.8 mm ($2'' \times 2''$) size and the ESL803 gold conductor is deposited on the LTCC substrate through a 325 screen mesh and an emulsion thickness of 20 μm. Next, the LTCC layers are stacked, laminated at 200 $bars$, 70° C for 10 minutes and finally fired up to 850°C in our belt furnace.

On the first view at the fired LTCC circuit, we see a lot of problems, that will be discussed in this section, such as the air bubbles in the substrate (red arrows) caused by the stacking and lamination errors, the deterioration at the edge of the circuit and the poor quality of deposited inks conductor (black arrows). Therefore, a dimensional measurement is made at different points of the circuit using our 3D optical measuring microscope shown in Figure 2.25. The substrate shrinkage in $x-y$ direction is calculated to a value of about 11 % relative to the circuit dimensions before firing, this value is different from that anounced by the manufacturer (15 ± 1 for ESL41110 tape).

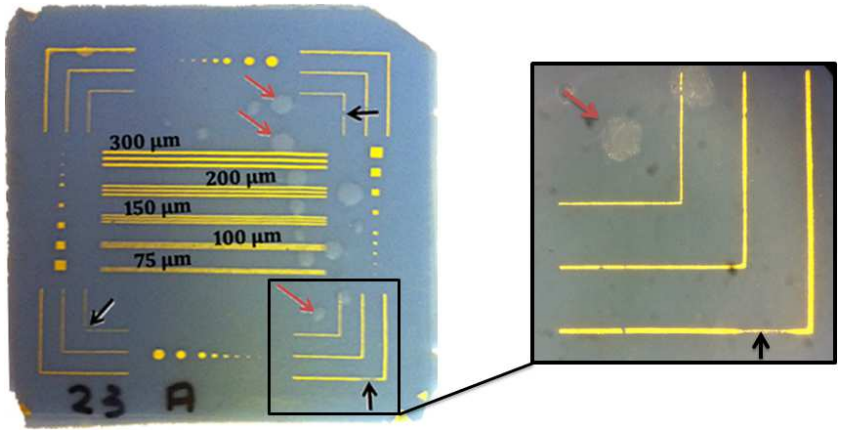


Figure 2.26: First print resolution test: poor quality deposited conductors (black arrows) and air bubbles (red arrows)

Now, to explain the screen printing errors, we refer to the cause and effect diagram (also knowing as FISHBONE or ISHIKAWA diagram) to identify and resolve these errors. This diagram is largely used in the industry in their production process quality work. Figure 2.27 illustrates

a FISHBONE diagram suggesting the potential errors of printing resolution process. As this diagram implies, the printing errors can be divided in five categories: environment, material, method, machine and operator. By checking operator and environment factors, our problem can be confined to the machine, material and method factors.

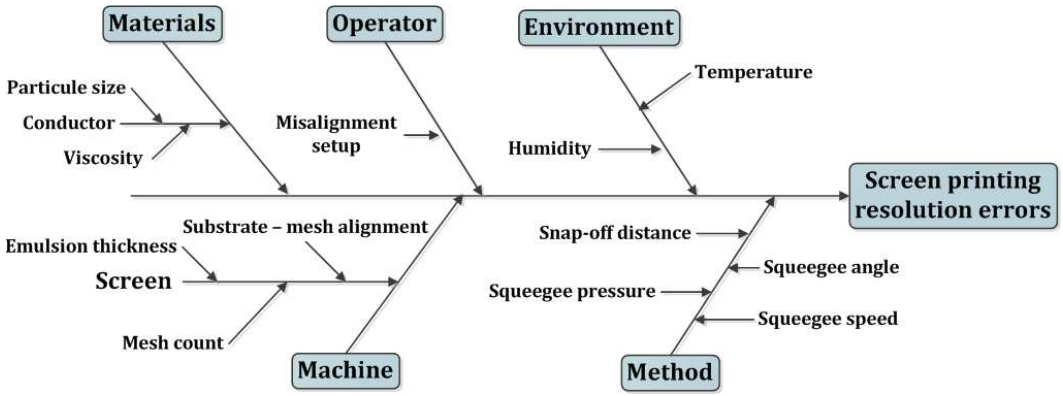


Figure 2.27: A cause and effect diagram for potential screen printing errors

First of all, we treat the errors from the machine. We made several tests by changing the screen and keeping the other parameters unchangeable. As it is well known, the screen count mesh, as well as the emulsion thickness, has an important effect on the deposited paste. A screen with higher mesh count will produce a print with better definition. The new used screen has a mesh count of 400 μm and the emulsion thickness is always 20 μm. By analyzing the results of these tests, the problem is regenerated and no improvement at the pattern definition is noted. Finally, the screen effect on the printed patterns is eliminated and the remaining quality problems can be related to other factors.

The second step is to analyze the materials used in screen printing process. This includes the LTCC substrate tape and paste inks. The shipped LTCC tape has normally two different sides: smooth (MYLAR side) and rough (other side). For better pattern definition, printing is recommended on the smooth side because the paste adhesion to the substrate is better [18]. The composition and characteristics of the paste are critical factors in screen printing process. The paste parameters are solid content, particle size and viscosity. These parameters depend on the manufacturer, only the viscosity can be increased by adding a thinner solvent, but it is very difficult to control, this is due to the sensitivity to several factors such as printing time, environmental parameters (temperature and humidity) and screen printer parameters (squeegee pressure, velocity and screen tension). To see the effect of conductor paste on the screen printing pattern resolutions, we made another test in which we replaced the ESL803 paste by the TANAKA gold conductor. The results are impeccable in terms of definition and thickness of the pattern. In this case, we decided to use the TANAKA paste for all the next LTCC circuits. With practice, and after the improvement of mechanical behavior of fired LTCC circuits, we discovered that the shrinkage value of the fired circuits was always different from that desired and was related to the TANAKA conductor paste.

For this reason, we return again to the cause and effect diagram to check the errors caused by the process and method. We went back to the ESL803 paste on the LTCC tapes and the screen printer settings were modified. After precise adjustment of snap-off distance (screen to substrate distance) and squeegee pressure of our screen printer, we finally obtain a good quality deposited ESL803 paste on the LTCC substrate. Figure 2.28 shows screen printed Coplanar Waveguide (CPW) structures using the ESL803 gold conductor before and after firing of LTCC tapes. After firing process, the center line width is about 600 μm and the space between center line and the ground is about 100 μm.

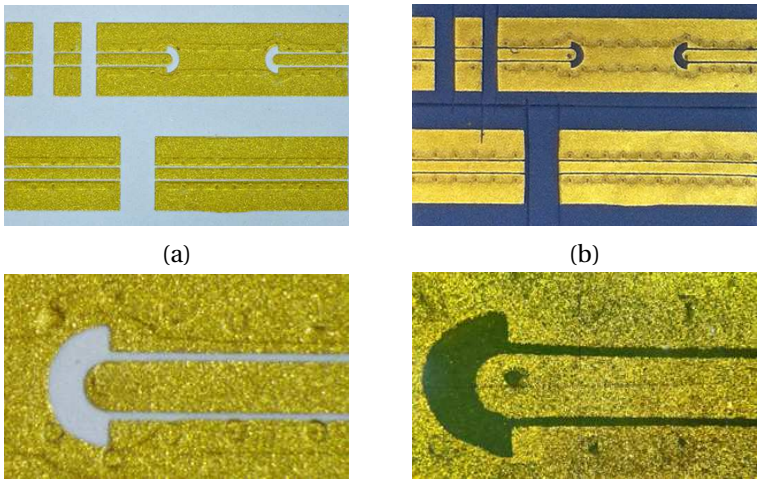


Figure 2.28: Printed CPW structures using ESL803 gold conductor on ESL41110 substrate before ((left) and after (right) firing process

2.4.2 Mechanical distortion

As we saw during the screen printing process validation in the previous section, the realized LTCC substrates are mechanically deformed after the firing process. This effect is due to several factors that start with the design stage and end by the firing process, via the stacking and the lamination steps. This section presents the mechanical behavior of some realized LTCC circuits, discuss the occurred problems and finally propose a solution required to avoid this deformation for high quality LTCC circuits.

To study the mechanical behavior of our LTCC circuits, we make the layout illustrated in Figure 2.29: it contains crosses that are distributed in a symmetrical way throughout the $x-y$ plane. This symmetrical distribution is required to avoid the non uniform shrinkage after the firing process of the LTCC circuit. The unfired circuit size is 50.8×50.8 mm and the distances between registration holes are 40 mm. The desired dimensions after firing are represented in Figure 2.29 (red text) where the others (black text) represent the scaled dimensions (+15 %) of the cross square. This scaling is necessary at the design step to compensate for the shrinkage of the circuit during the firing cycle.

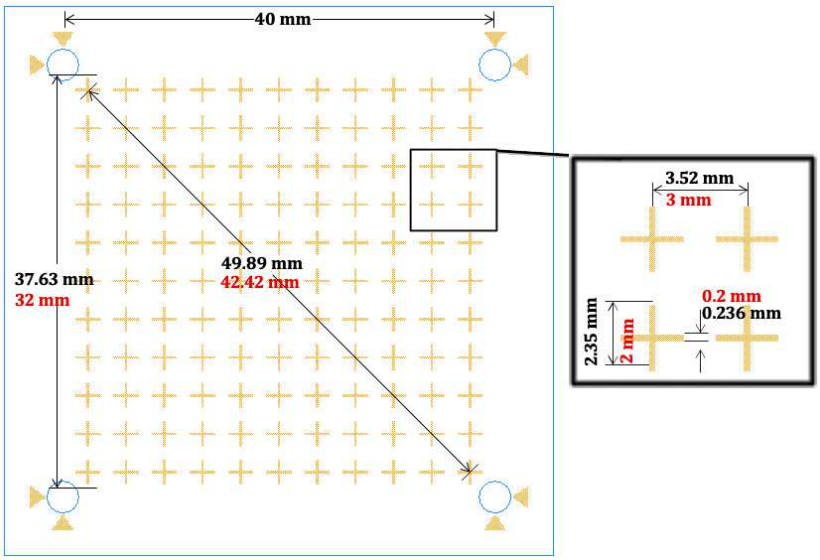
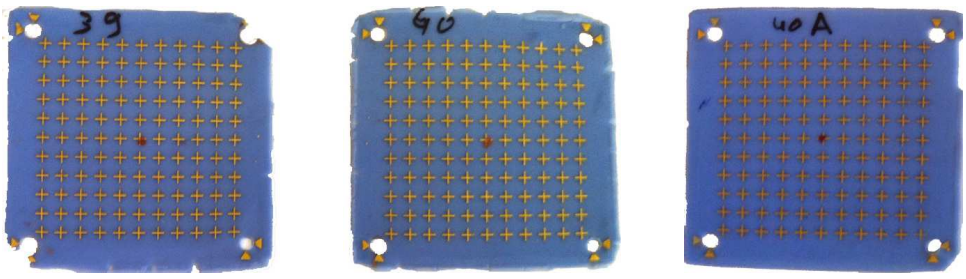


Figure 2.29: Designed patterns for mechanical verification of LTCC circuits

Once the design is completed, the LTCC layers are cut in the desired size using a blade tool. At the same time, the mask required for the screen printing is generated and the 325 mesh screen is prepared. Firstly, to see the reproducibility of the distortion on our realized LTCC tests, we made three separate circuits, each composed of five ESL41110 LTCC layers. Due to its good definition as discussed in the previous section, the TANAKA paste is used to pattern the crosses on the substrate by screen printing operation. The printed patterns are dried in our box oven at 120°C. For perfect precision, the registration holes are created after printing by the laser machine and then the layers are manually stacked using the three pin stacking tools. On the third circuit (Figure 2.30-(c)), the adjacent layers are rotated by 90° prior to stacking. The aim of this is to diffuse the shrinkage in all directions because the LTCC substrate is tape casted only in one direction. Next, each circuit is uni-axially laminated at 200 $bars$, 70° C for 10 minutes. Finally, the laminated circuits are ready to be fired up to 850°C in the belt furnace.



(a) (b) (c)

Figure 2.30: Realized LTCC circuits with crosses patterned on five ESL41110 layers

As shown in Figure 2.30, the circuits are mechanically deformed especially at the edges. After the firing process, the circuits dimensions are measured by the optical microscope at different

positions in x and y directions as shown in the Figure 2.31. We note also that all LTCC layers are inspected and checked after the screen printing process, and then no errors and deformations are seen except in the tolerances related to the process itself.

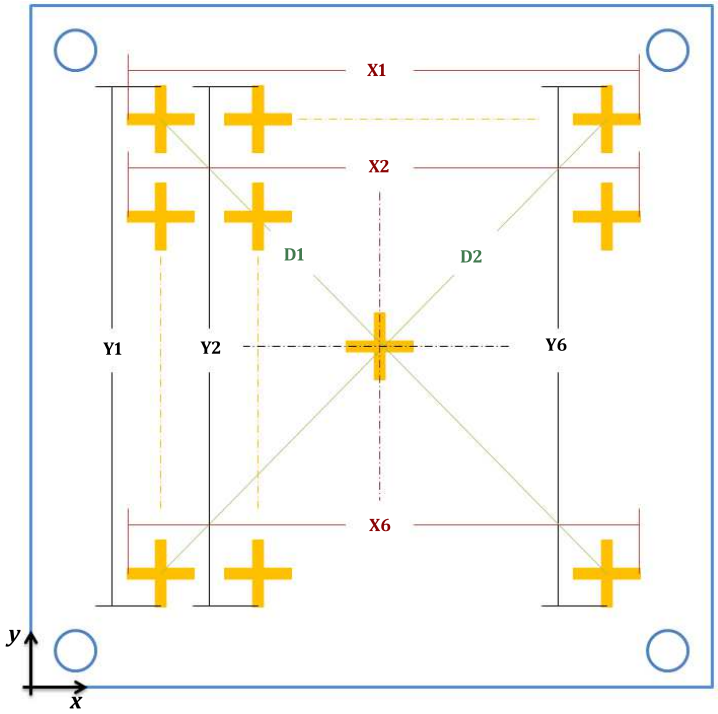


Figure 2.31: Measured positions of the fabricated circuits after firing process

The two graphs given in Figure 2.32 illustrate the measured positions in the x and y directions. The first point to note is the gap between the dimensions of the designed (blue) and the realized test circuits (others). This gap is due to the shrinkage value which is different from that used at the design step (+15 %). Another phenomenon we can observe from Figure 2.32 is that the distortion increases at the edge of the circuits (X1, X6, Y1 and Y6 positions). This distortion is very important and exceeds 800 μm on the circuit "40-A" (Y6).

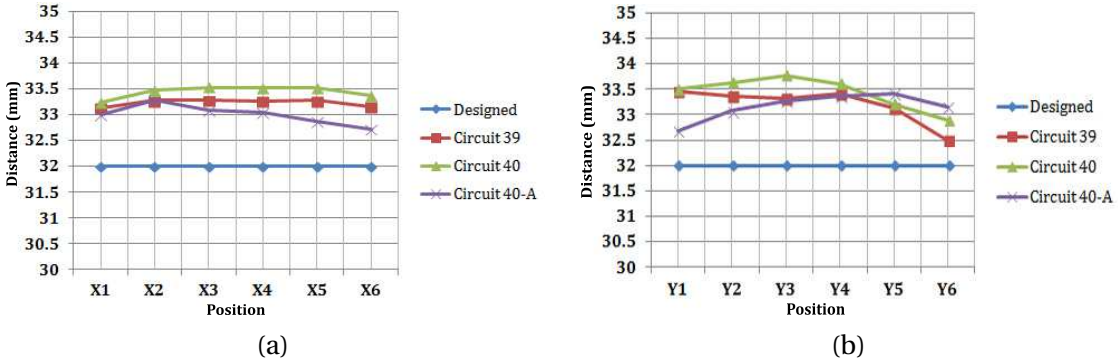


Figure 2.32: Dimensional measurement of the distortion on the fabricated LTCC circuits: (a) Horizontally and (b) vertically

The analysis of this distortion is carried out by the study of the manufacturing parameters during the processing of the circuits. By checking the design layout and the patterned crosses after screen printing, these factors can be eliminated. As illustrated in Figure 2.33, the origin of the problem can be confined at the stacking, lamination or firing steps.

(a) (b) (c)

Figure 2.33: Potential origin of the mechanical distortion on the LTCC circuits: (a) Stacking step. (b) Lamination process. (c) Firing process

To simplify the identification, we start with analyze of the firing process because we believed that the firing profile of the belt furnace is not exactly that used by ESL laboratory and thus resulting in a deformation of the circuits. For this reason, we made another circuit named "42" with the same processing parameters of the previous circuits and firing it in the box furnace programmed with the exact firing profile proposed by ESL. After circuit measurement, the distortion still appeared at the edges and no change was noticed.

The second step was to verify the alignment fixture. Normally, a pin fixture produces a maximum error of 50 μm on the manually stacked LTCC layers, but in our tests, the error is very important and exceeds 500 μm. A dimension measurement is achieved to verify if the fixture is deformed during the previous laminations and thus no deformation was remarked. In addition, we check the parallelism of their surfaces, and then no important effect was noticed. Returning again to the previous fabricated circuits, we found that the diagonals measured as in Figure 2.31 are not equal and one diagonal is always greater than the other. Table 2.3 shows the measured diagonals $D1$ and $D2$ while $D1$ represents the largest dimension.

Table 2.3: Measured diagonals of LTCC circuits

LTCC circuit	**Designed** $D\ (mm)$	**Measured** $D1\ (mm)$	**Measured** $D2\ (mm)$	**Measured** $D1-D2$(mm)
39	42.42	44	43.39	0.065
40	42.42	44.31	44.08	0.23
40-A	42.42	43.9	43.73	0.17
42	42.42	44.665	44.29	0.37

As shown in Table 2.3, the difference between the measured diagonals is up to 370 μm as in the circuit "42". This difference is caused by the lack of the fourth pin in the alignment fixture. In order to validate this argument, another test (43) composed of six ESL41110 layers which are screen printed with the same patterns was performed. After layer stacking, the diagonal

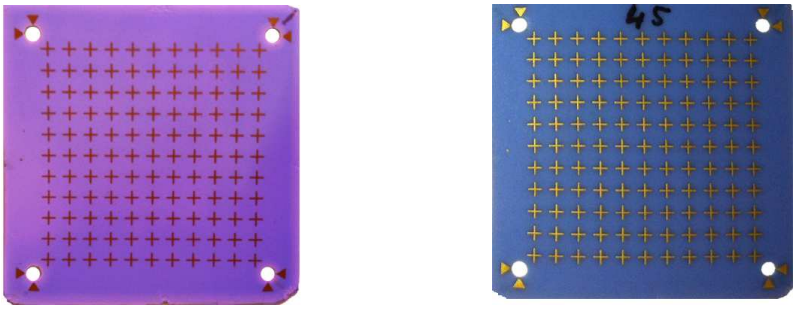
$D1$ is marked on the side where a pin is missing in the fixture. Next, the circuit is pressed an finally fired in the box furnace. Table 2.4 shows the measured diagonals performed on each layer during stacking and on the top layer after both the lamination and firing process.

Table 2.4: Measured diagonals of realized circuit "43"

LTCC circuit	**Measured** $D1\ (mm)$	**Measured** $D2\ (mm)$	**Measured** $\lvert D1-D2\rvert\ (mm)$
Layer 1	49.83	49.87	0.04
Layer 2	49.825	49.81	0.015
Layer 3	49.78	49.87	0.09
Layer 4	49.825	49.79	0.035
Layer 5	49.835	49.825	0.01
Layer 6	49.805	49.82	0.015
After Lamination	50.24	50	0.24
After Firing	43.92	43.73	0.19

From this table, it is obvious that after lamination the diagonal D1 (no side pin) is 240 μm larger than D2 and thus, this error is transferred to the fired circuits resulting in a mechanically distortion. Normally, it is possible to resolve this problem by the use of four pin alignment fixture, but this solution is not recommended because the pins may limit the expansion of the substrate at the corners during lamination, and can generate another form of distortion. For this purpose, we have developed a new technique without pin fixture for better mechanical performance during lamination. The principle consists of sealing the stacked LTCC layers at the corners using Iso Propyl Alcohol (IPA). Next, the sealed layers are placed between two stainless steel plates and then pressed without the alignment pin fixture.

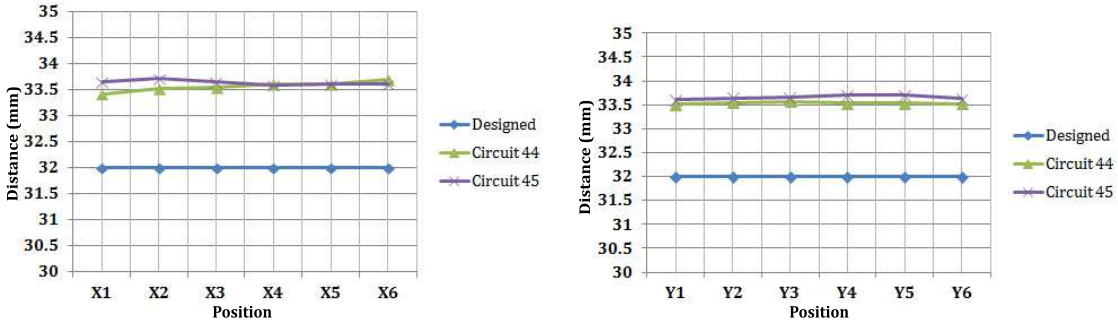
To validate the accuracy of this method, two new circuits were fabricated each formed of six ESL41110 layers patterned by the cross forms using the TANAKA paste conductor. The layers are sealed after stacking, pressed and then fired in the box furnace. Figure 2.34 shows the laminated and fired circuit "45" using the new technique described above. With a simple visual inspection, the LTCC template is very clean and no deformation of the circuit is observed.



(a) (b)

Figure 2.34: Six LTCC layers with cross patterns: (a) Laminated without pin fixture. (b) Fired in the box furnace

Finally, the circuits are measured in x and y positions as shown in Figure 2.31. Figure 2.35 shows that the fabricated tests behave in a uniform way and the distortion observed in the previous circuits is removed.



(a) (b)

Figure 2.35: Dimensions measurement of the distortion on the circuit "45": (a) Horizontally. (b) Vertically

2.4.3 Substrate shrinkage problems

As discussed in the co-firing process of LTCC substrate in section 2.3.7, the laminated LTCC circuits shrink during firing at the end of the burn-out stage, in order to give a mono-bloc and dense LTCC circuit. Thus, the circuit size must be uniformly decreased in both the lateral and vertical planes. Normally, the shrinkage value depends on the material compositions and is different from one tape to another. Although the shrinkage value provided by the supplier is theoretically correct, several factors can affect this value and, as in the previous fabricated LTCC circuits, a shrinkage value different from that announced by the manufacturer can be obtained. Therefore, it is very important to control the shrinkage of the LTCC circuits especially for RF applications as in our case, because the variation of circuit dimensions led to a shift of the desired operating frequency.

Simply, the shrinkage value in one direction (x, y or z) is calculated by Equation 2.5:

$$\text{Shrinkage (\%)} = \frac{\text{Before firing dimension} - \text{After firing dimension}}{\text{Before firing dimension}} \times 100 \tag{2.5}$$

It is necessary to note that the circuit dimensions before firing represents the measured data after the lamination step and are not the size of LTCC tapes at the preparation step, because the circuit size increases under pressure in x and y direction while the substrate thickness decreases in z direction.

Table 2.5 shows the shrinkage values given by ESL of the LTCC tapes ESL41110 and ESL41060. We note that the ESL41060 is a high permittivity LTCC substrate ($\varepsilon_r = 18$) necessary for some RF applications.

Table 2.5: Shrinkage values of our LTCC substrate from ESL

LTCC Tape system	x-y	z
ESL41110	15 ± 1 %	16 ± 2 %
ESL41060	9.5 ± 0.5 %	15 ± 1 %

In the previous sections (section 2.4.1 and section 2.4.2), we presented several manufactured LTCC tests using the implemented LTCC process in the laboratory. Beyond the discussed problems, all of these circuits, which are composed of the ESL41110 tape, present a non controlled shrinkage after circuit firing. The calculated values are not conform to that mentioned in Table 2.5 and vary from one circuit to an another. It is clear from Figure 2.36 that the measured shrinkage in x and y directions at the cross patterned circuits is not uniform and distortion errors appear at the edges of LTCC circuits. After distortion error elimination using the new lamination technique discussed in the previous section, quasi-linear values of shrinkage are obtained as in the case of circuits "44" and "45" (solid lines), but these values are always out of the range.

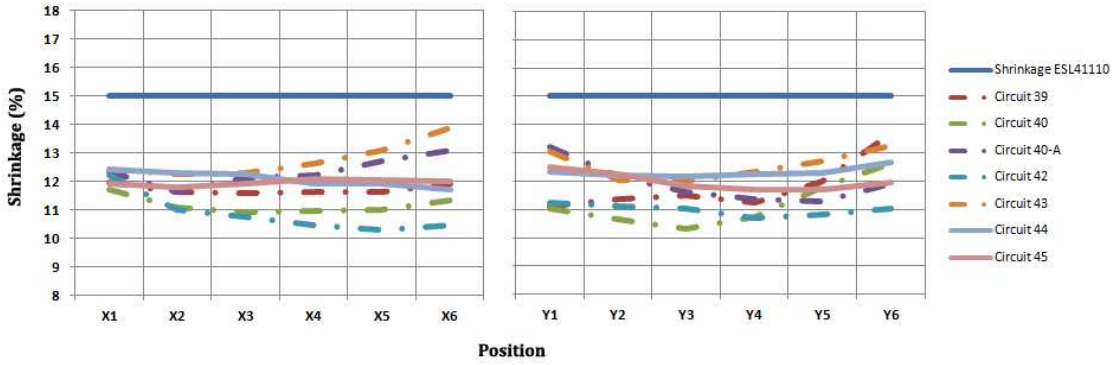


Figure 2.36: Measured shrinkage values of LTCC circuits with cross patterns in x and y directions

Shrinkage can occur at several steps in the processing of LTCC circuit. At the production, the composition of materials as well as the tape casting method strongly influences the shrinkage values. It is important to indicate that the storage time and temperature of LTCC materials also can affect the shrinkage, but our interest in this section is to identify the shrinkage problems caused by layout load and processing factors of LTCC circuits.

Beyond the layout influences on the LTCC circuit shrinkage, the shrinkage can be affected by all the fabrication process steps. It may be caused during blanking and cutting of LTCC tape, mylar removal and substrate handling. The via drilling and filling as well as the paste patterning can change the desired shrinkage value. The lamination parameters also adjust the shrinkage especially in the case of uniaxial lamination. Finally, the most important shrinkage variation occurs during the firing process, as well as the used setter that plays an important role in the circuit shrinkage during firing.

After this enumeration, the shrinkage behavior of our LTCC circuits is studied by checking of all these factors. In order to simplify the problem analysis, Figure 2.37 shows the next fabricated circuits as well as the suited actions to identify the shrinkage problems.

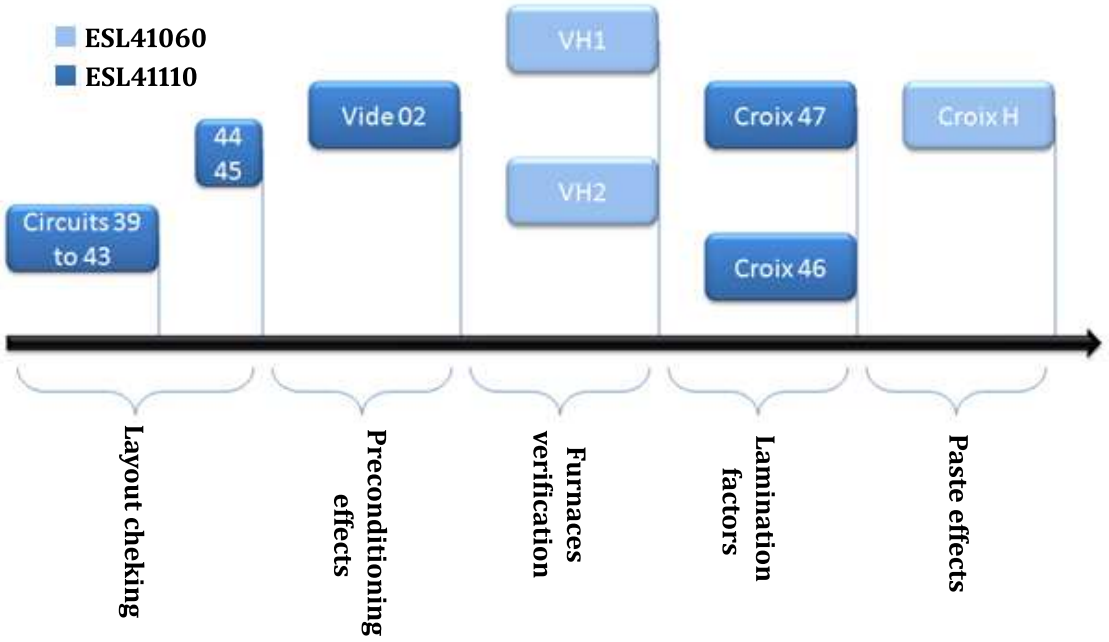


Figure 2.37: Summarize of the realized tests and actions to resolve the shrinkage problem

2.4.3.1 Layout-checking

First, we studied the effect of the design process on the substrate shrinkage value. This study includes the metal distribution over a layer, the metal load per layer and the number of layers. The fabricated LTCC circuits with crosses (circuit 39 to 45) described in the previous section respond to these requirements. By referring to Figure 2.36, where is given the shrinkage of the symmetrically distributed cross patterns, the design factors are eliminated, and the problem is due to the manufacturing process of LTCC technology.

2.4.3.2 Preconditioning effects

To eliminate the effect of the carrier film after tape preparation, a tape layer relaxation and stabilization step is introduced by heating the blanked LTCC tapes in an oven at 80° C for 30 minutes. The first test circuit is composed of six empty ESL41110 layers. The empty layers are used in order to avoid the paste solvent influences and drying cycles on the substrate shrinkage. As usual, the LTCC layers are cut, stacked after stabilization, laminated at the recommended parameters and finally fired in the box furnace. As shown in Figure 2.38, the circuit "vide 2" presents some errors. The air bubbles are caused by the bad bonding between layers caused by a too high temperature during lamination (the temperature of bottom plate

of the press machine increases up to 71° C during 2 minutes). Another defect which appears at the circuit is that the edge (bottom left) is deformed because of a displacement of the circuit outside the setter during the firing process. This is due to high pressure of the emitted gas inside the furnace that lacks a ventilation system.

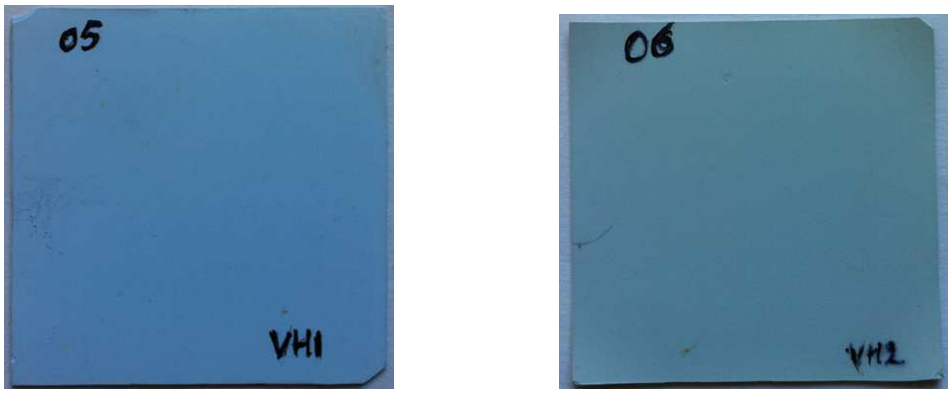
Figure 2.38: The LTCC circuit "vide 2" composed of six empty ESL41110 layers for preconditioning effect verification on the substrate shrinkage

Now, returning to our shrinkage problem, the circuit dimensions were measured and the shrinkage value was calculated to be 13.6 – 15.3 % in x, 12.5 – 13.3 % in y and 14 – 15 % in the z direction. These results are encouraging when compared to the previous realized tests, because the result is correct in z direction, while the problem still remains (but is less important) in the x and y directions. We note that the important variation in x is due to the circuit deformation. Finally, to conclude, it is clear that the preconditiong after LTCC cut improves the shrinkage value but these values are always different (in x and y directions) as compared to what is anounced by ESL (see Table 2.5).

2.4.3.3 Firing furnace verification

To go on with our problem analysis, next we change the LTCC material substrate in order to see if the problem comes from the furnaces (box and belt furnaces) or the material itself. The used material is now the ESL41060 with shrinkage values listed in Table 2.5. The new circuits are prototyped in two versions for firing in the both the box and belt furnaces. Each circuit is composed of six LTCC layers which are stabilized at 80° C for 30 minutes. Next, the two circuits are stacked and then uniaxially laminated. To avoid the appearance of air bubbles such as was seen in the previous circuit, the temperature during the lamination step is reduced to 68° C while the pressure and the time remain unchanged. Finally, one of the circuits is fired in the conveyor belt furnace while the other is fired in the box furnace with the same firing profile for ESL41060 used by ESL. Figure 2.39 shows the two fabricated circuits named "VH1" and "VH2" which are fired in the belt and box furnace respectively.

After firing, the circuit dimensions are measured at different positions in x, y and z directions.



(a) (b)

Figure 2.39: Fired LTCC circuits composed of empty ESL41060 material: (a) In belt furnace. (b) In box furnace

The graph below illustrates these measured data with min and max values. The red markers represent the shrinkage values of the circuit fired in the belt furnace "VH1", while the green markers are those for the circuit "VH2" fired in the box furnace.

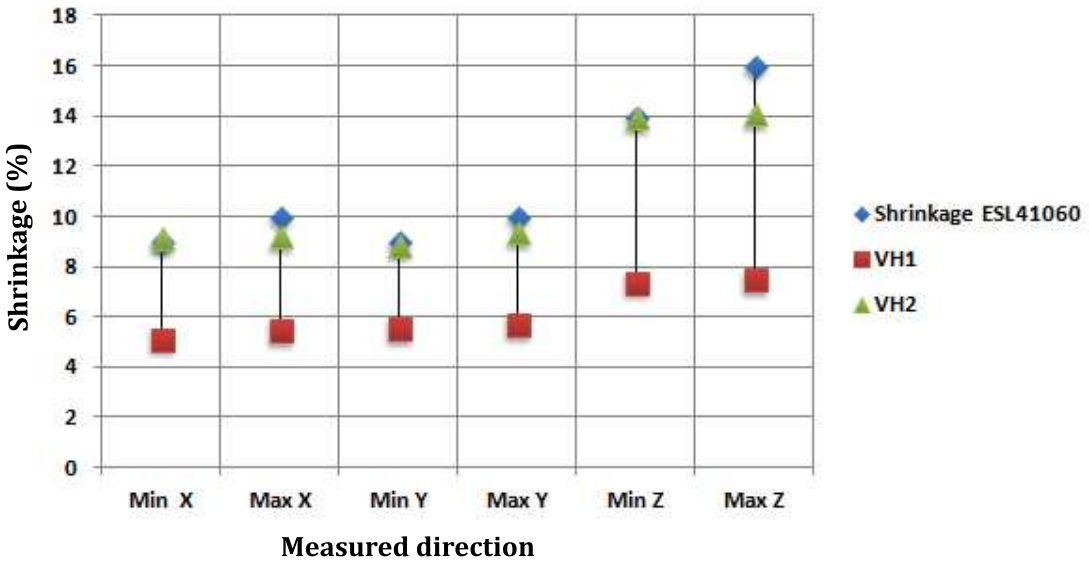


Figure 2.40: Shrinkage values of circuits "VH1" and "VH2" in x, y and z directions

As shown in Figure 2.40, the shrinkage values in all directions of the circuit "VH1" are very far from ESL values, while those for "VH2" (green markers) are very close to the ESL41060 shrinkage values. The color difference between the two fired circuits in Figure 2.39 shows that the firing process of circuit "VH1" in belt furnace is incomplete or rather the burn-out stage of the firing profile of our belt furnace is not conform with this LTCC material. Therefore, firing of LTCC circuit in a box furnace is correct and the shrinkage problem is not related to the furnace itself.

2.4.3.4 Lamination and paste effects

As discussed in the previous section, the firing process in the box furnace is normal and thus the non controlled shrinkage depends on the lamination and screen printing process. The shrinkage values of the presented circuit "VH2" is ideal. To identify the probable lamination errors, we start from the circuit "VH2" to analyze our problem. Neglecting the material compositions of ESL41110 and ESL41060, which can result in different shrinkage values, Table 2.6 compares the physical properties and the processing parameters of the two circuits "vide 2" presented on Figure 2.38 and "VH2" presented above.

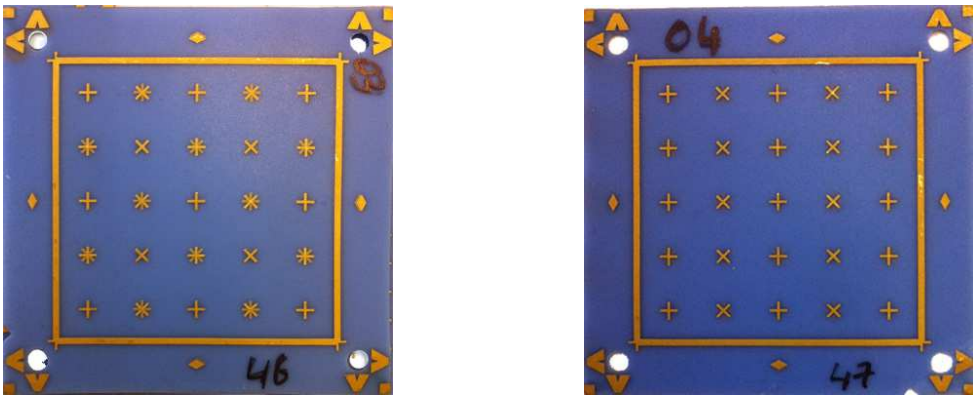
Table 2.6: "Vide 2" and "VH2" circuits comparison

	Vide 2	**VH2**
LTCC material	ESL41110	ESL41060
number of layers	6	6
Substrate thickness after lamination	$517-530\ \mu m$	$765-775\ \mu m$
Substrate thickness after firing	$440-450\ \mu m$	$690-700\ \mu m$
Lamination temperature	$70-71^{\circ}\ C$	$68-69^{\circ}\ C$
Firing profile (box furnace)	ESL41110	ESL41060

From Table 2.6, we see that the lamination temperature is different. In addition, the circuit "VH2" is thicker than "vide 2" due to the layer thickness of ESL41060 which is at about 130 μm while the ESL41110 layer thickness is 106 μm. The effect of the lamination process on the circuit "vide 2" seems clear. Therefore, it is necessary to take care of the lamination parameters, especially when the circuit is uniaxially pressed as in our case. The conductor areas are more influenced by the higher pressure than the substrate material and this leads to less shrinkage values at the conductor and a larger shrinkage value at the substrate. The most important parameter during lamination is the temperature which causes flowing of the tape, and changes the material density, which then results in high shrinkage variations in all directions. For this reason, it is required to control the temperature when using uniaxial lamination. This temperature must be selected according to the substrate thickness, and must be decreased in the case of thinner LTCC circuits.

After this discussion, we return to the ESL41110 tape taking into account the new factors described above and testing at the same time the paste influence on the substrate shrinkage. For these new prototype tests, the number of layers is increased to seven; a new layout with crosses, rotated crosses and stars is designed for circuit patterning. The same processing parameters used in the previous circuit "VH2" are applied on the two next circuits. The ESL41110 layers of these two circuits are patterned using the TANAKA (croix 46) and ESL803 (croix 47) pastes (see Figure 2.41). The drying cycle after paste deposit is $80^{\circ}\ C$ during 10 *minutes*.

After firing, the circuits are inspected and mechanically measured. The shrinkage values in x, y and z directions are represented on Figure 2.42. As shown in this figure, the x and y



(a) (b)

Figure 2.41: Influence of the paste on the LTCC substrate shrinkage: (a) TANAKA paste. (b) ESL803 paste

shrinkage of the circuit "croix 46" (red markers) are below the shrinkage limit of ESL41110 tapes (blue markers). Only the shrinkage values of the circuit "croix 47" (green markers) are close to the min limit (14 %) of ESL41110 tape in x and y directions and very close to the range in z direction.

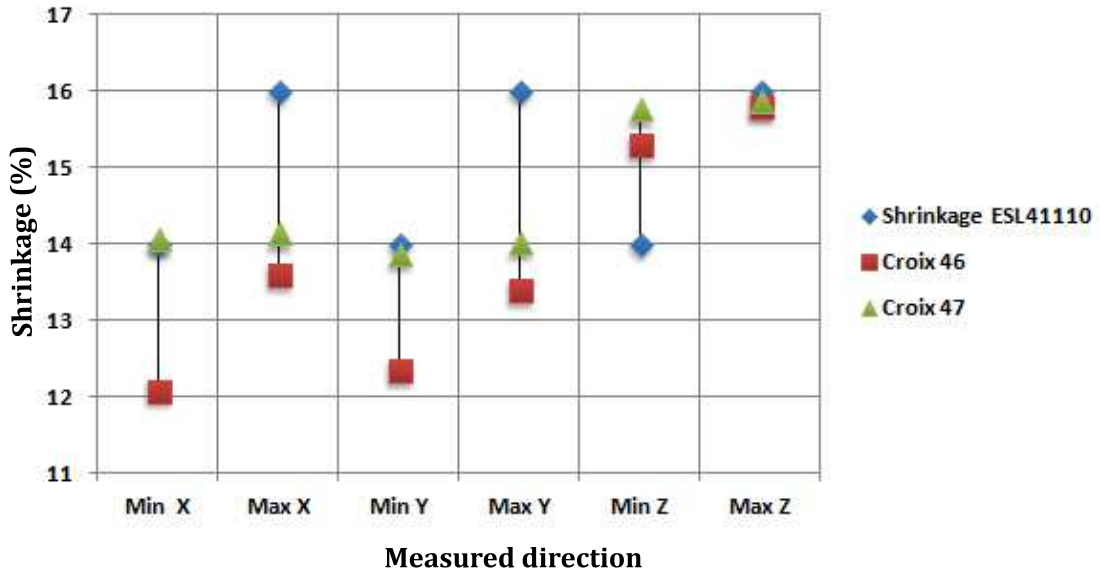


Figure 2.42: Shrinkage values of circuits "croix 46" (TANAKA) and "croix 47" (ESL803) in x, y and z directions

To conclude, only the ESL803 paste must be used because it is compatible with the ESL tapes. In order to confirm this statement, we made another circuit with the same crosses but patterned on six ESL41060 layers using the ESL803 paste. The LTCC layers are processed in the same way as the previous circuits except the firing profile is changed. Figure 2.43 illustrates the realized circuit named "croix H". The shrinkage value of this circuit is very close

to that listed in Table 2.5 and varying between 8.9 and 9.5 % in x and y directions, while the z shrinkage is at about 15.6 %.

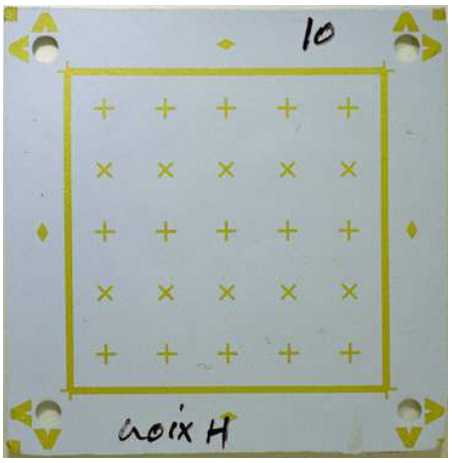


Figure 2.43: Fabricated circuit for validation of ESL803 paste effect on shrinkage behavior of ESL substrate

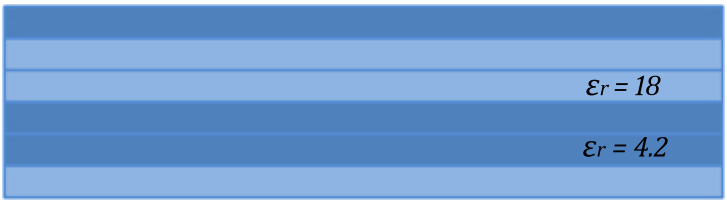
Finally, to end this section, and returning back to Figure 2.37, we summarize the suited approach for resolving the shrinkage problem. First of all, the important non uniform shrinkage measured on the previous circuits with cross forms (circuits 39 to 43) is related to the distortion problem. After distortion elimination, the layout is checked and the adjacent layers are rotated by 90° in circuits "44" and "45" to compensate for the shrinkage in the tape direction. The shrinkage becomes uniform but still out of the range. Next, the preconditioning step is inserted in the manufacturing process; the shrinkage value is slightly improved. Then, we check the firing furnaces using the substrate material ESL41060, they result in very close shrinkage values on the circuit "VH2" fired in the box furnace. With these results in hand applying the same used parameters in the processing of the circuit "VH2", we made two other circuits using the ESL41110 materials and changing the paste. The circuit patterned with the ESL803 paste "croix 47" presents desired shrinkage values. Finally, to validate this statement, the new cross pattern is deposited again using the ESL803 conductor on the ESL41060 LTCC substrate (Croix H). The shrinkage values are in the range of those given by ESL.

2.4.4 High permittivity material integration

The demand of high level and compact RF packages has led to an evolution in the integration technology of passive elements such as capacitors, inductors and filters. One of the most great benefits of LTCC technology is the possibility to integrate passive elements using high permittivity, capacitive and ferromagnetic substrate materials. DUPONT, HERAEUS and ESL suppliers offer LTCC materials with high permittivity values up to 250. Only the American manufacturer ESL offers ferromagnetic tapes with permeability values up to 500. In our laboratory, besides the ESL41110 material, we have introduced the ESL41060 LTCC tape (ε_r = 18) for capacitive and decoupling functions. In this section, we present the main difficulties

encountered with ESL41060 material integration inside the ESL41110 substrate material.

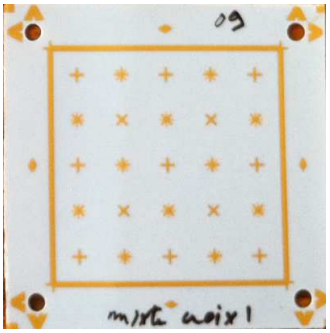
The key consideration that one must to take into account when integrating different substrate materials is the shrinkage control of different substrate materials, which is strongly related to the selected firing profile. The fabricated tests concern the integration of ESL41060 layers inside the ESL41110 materials. As shown in Figure 2.44-(a), the high permittivity layers are mixed inside the low permittivity layers. Three circuits were manufactured using the recommended processing parameters. The two first "mixte v1" and "mixte v2" are composed of empty layers while the third (mixte croix 1) is composed of cross patterned layers. The belt furnace is used for "mixte v1" circuit firing while the "mixte v2" and "mixte croix 1" are fired in the box furnace with the exact ESL41060 firing profile. We note that the shrinkage values provided by the manufacturer of ESL41110 and ESL41060 materials is 15 ± 1 and 9 ± 1 in the x and y directions respectively.



(a)

(b)

(c)



(d)

Figure 2.44: High permittivity ESL41060 material integration in ESL41110 substrate: (a) Circuit geometry. (b) Empty layers fired in belt furnace. (c) Empty layers fired in box furnace. (d) Cross patterned layers fired in box furnace

The shrinkage values of these three circuits are illustrated in Figure 2.45 relative to the two LTCC material shrinkages in all directions. As a result, the circuit "mixte v1", fired in the belt furnace, has insufficient shrinkage due to the incomplete circuit burnout. The firing profile of our belt furnace is not compatible with those materials. The others (fired in the box furnace) present shrinkage values close to that of ESL41060 materials. To conclude, the firing of mixed circuits is only valid with the box furnace and the shrinkage behavior is adapted with one of the two shrinkages of ESL41110 and ESL41060 tapes.

In some cases such as decoupling capacitors, there could be a need to use one high permittivity

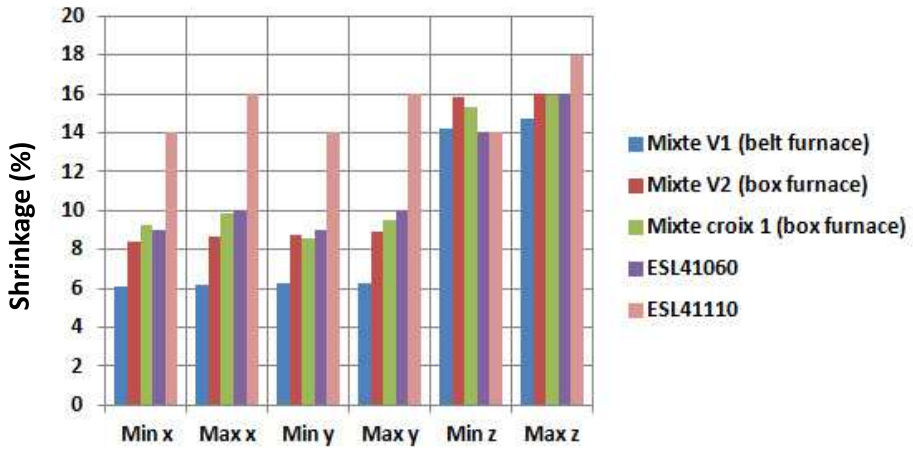


Figure 2.45: Measured shrinkage of mixed LTCC circuits in x, y and z directions

layer inserted between several layers of low permittivity substrate. For this reason, in the next two circuits we integrate (at the bottom of the circuit) one ESL41060 layer in six ESL41110 layers and fire in the box furnace with different firing profile. Figure 2.46 shows these two new circuits fired with ESL41060 (left) and ESL41110 (right) profiles.

(a) (b)

Figure 2.46: Integration of one ESL41060 layer in six ESL41110 layers: (a) With ESL41060 firing profile. (b) With ESL41110 firing profile

In contrast to the circuit presented in Figure 2.44, these circuits are mechanically deformed and present a strong camber at the edge of the circuits. This effect is due to that the proportion of the two material is different and the number of mixed layers is not equal. To avoid this effect, a solution for this problem consists in using the high permittivity material as small inserts and place it in cavities created in the low permittivity substrate (Figure 2.47).

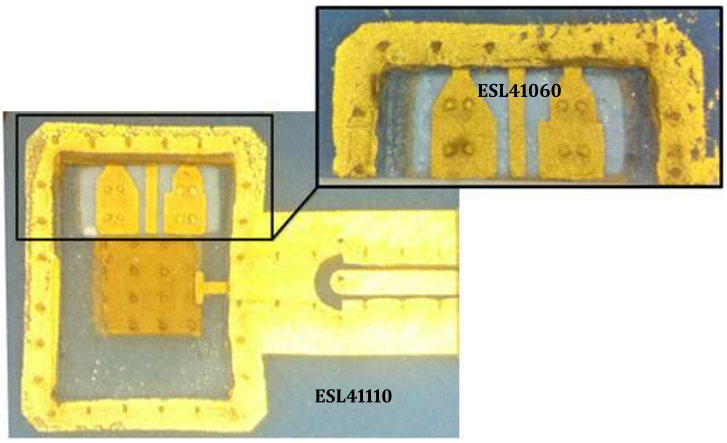


Figure 2.47: ESL41060 used as insert in ESL41110 material to create decoupling capacitors

2.4.5 Via fill difficulties

The drilled vias of LTCC tape are filled by ESL802 gold conductor paste using conventional thick film screen printer through meshed screen and emulsion. The quality of the fill is important because it affects the vertical interconnection between layers. The problems that we will discuss in this section concern the misalignment of the fill, and the insufficient paste quantity applied to the vias. Figure 2.48 shows the first via fill test composed of six ESL41110 layers. The via diameter is between 240 μm and 400 μm and horizontal conductor lines are used at different layers to verify by electrical DC tests the via interconnection.

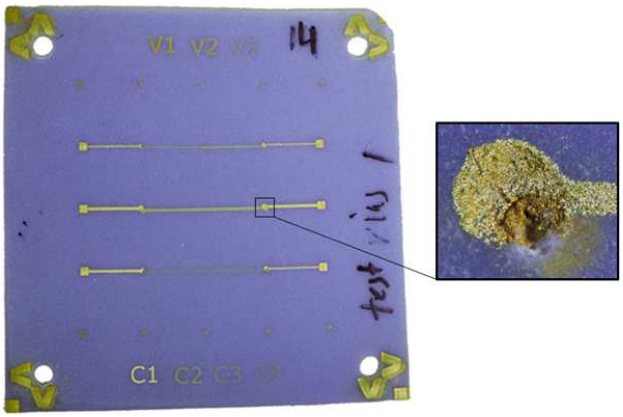
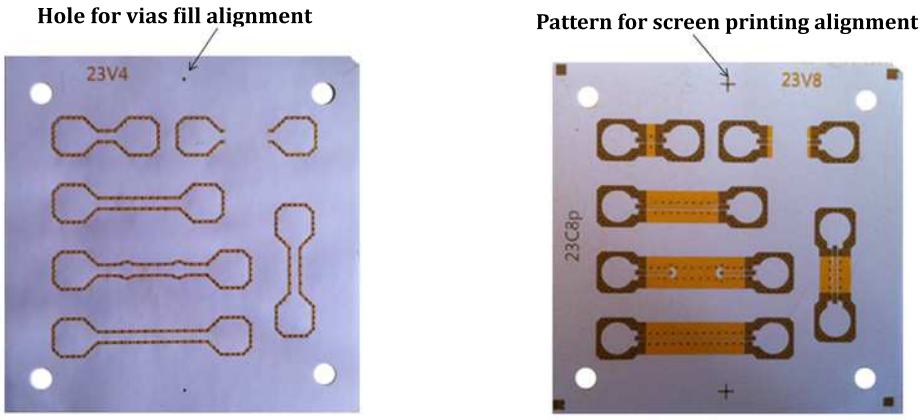


Figure 2.48: Via fill problems: misalignment and incomplete via fill

The misalignment is due to the bad screen to substrate alignment. With the optical camera mounted in our system, there is no possibility to view and align directly both via holes in the screen and the substrate. The alignment process is made by patterns located around the registration holes. These patterns are not efficient for via fill and are valid only for screen printing process. To achieve an accurate alignment we update the pattern for both vias fill and screen printing process as shown in Figure 2.49.



(a) (b)

Figure 2.49: Via fill (a) and screen printing (b) misalignment solution

The quantity of the paste transferred to via is important because an insufficient paste may result in a bad contact between the lines and vias and then degrade the electrical signal, especially at very high frequencies. To avoid the incomplete metalization of the vias, the via diameter must be chosen according to the layer thickness (*via diameter* = 3× *substrate thickness* max). The use of the screen instead the stencil during via fill process also affects the amount of paste transfered to via due to the mesh of the screen. To obtain better results in this case, the paste viscosity and the pass number during the process are adjusted. Figure 2.50 shows a successful filled via (before firing) through a 325 $mesh$ screen. The via diameters are 170 μm, which equal to 1.6 × *layer thickness* (the layer thickness of ESL41110 is about 106 μm before firing). The spacing between vias is about 450 μm.

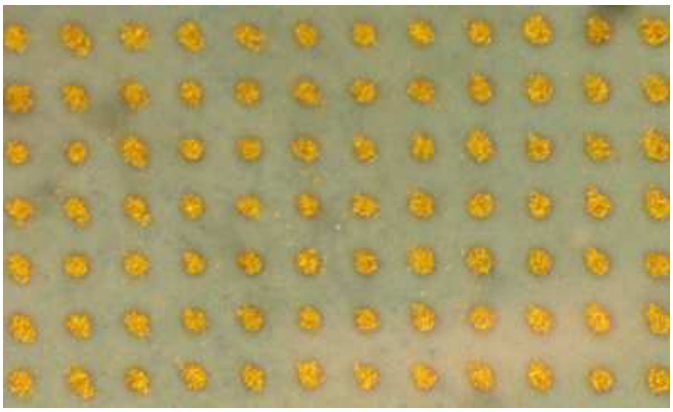
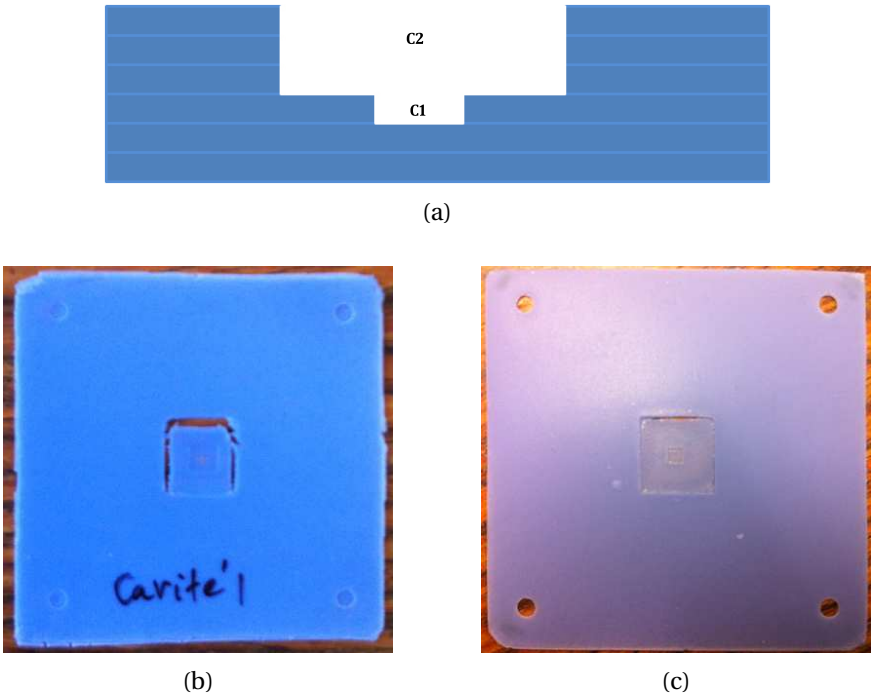


Figure 2.50: ESL802 gold conductor via fill using a 325 mesh screen on ESL41110 LTCC substrate. The via diameter is 170 μm, the via spacing is 450 μm and the substrate thickness is 106 μm

2.4.6 Cavity deformation

The LTCC technology allows the creation of different 3D shapes such as cavities and channels. In RF applications, open cavities are necessary for the placement of semiconductor chips in order to minimize the wire bond length and thus improve the performance of the RF signal. At the lamination step, the cavity may deform because the pressure strength at the cavity edge is relatively high. To balance this high pressure, the cavity must be filled before lamination by a fugitive material that disappears during firing. Figure 2.51 shows two ESL41110 tests each containing two cavities "C1" and "C2" with dimensions of $1.85 \times 1.85mm$ and $8.75 \times 8.75mm$ respectively. The first circuit is laminated without the fugitive material while the second is filled with the ESL49000 fugitive tape.



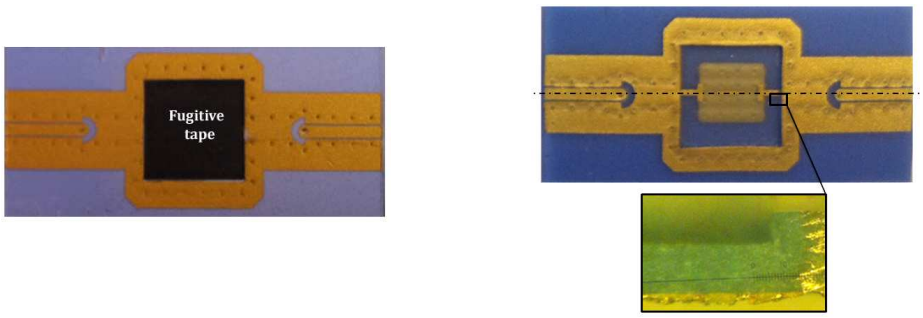
(a)

(b)

(c)

Figure 2.51: Open cavity test on six ESL41110 layers: (a) Circuit geometry. (b) Circuit laminated without fugitive tape. (c) Circuit laminated with ESL49000 fugitive tape

As these figures show, the cavities are deformed in the first circuit (Figure2.51-(b)) while the second (Figure2.51-(c)) is less deformed due to the use of the fugitive material during the lamination. The fracture appeared in the cavity "C2" is related to the substrate material thickness under the cavity (300 μm before firing). The recommended thickness used by LTCC circuit manufacturers is between 400 μm and 500 μm which correspond to a minimum of 4 and 5 layer count on ESL41110 substrate. Figure 2.52 illustrates one circuit where the recommendation cited above was taken into account. The circuit is composed of eight ESL41110 layers and the cavity is created on the top four layers.



(a) (b)

Figure 2.52: Fabricated open cavity on eight ESL41110 layers: (a) Before firing with ESL49000 fugitive tape. (b) After LTCC circuit firing

2.4.7 Fired LTCC circuit cut

Initially, a laser is used to cut the fired LTCC circuits. The process is slow and the laser strongly affects the LTCC surface due to the glass presence in the LTCC material. In addition, the high power delivered by the laser results in burning marks at the circuit edges. To fix this problem, the LTCC circuits are precut before firing using a heated blade tool. After firing, the parts of the LTCC circuit are singulated by manual breaking. The edges of the parts are blunt, but their quality is better than those cut by laser. In order to improve the edge quality, the parts are smoothed by a polishing machine. The two examples illustrated on Figure 2.53 show a laser (left) and broken (right) fired LTCC circuits. The black arrows on Figure 2.53-(a) show the fracture of the circuit edge during laser singulation while the second shows a better singulation quality. The circuit is manually precut before firing (Figure 2.21) at the part edges using a 80°C heated blade.

(a) (b)

Figure 2.53: Cut of fired LTCC circuit: (a) Using a laser machine. (b) Using a heated blade before firing

2.4.8 Circuit fragility and mechanical constraints during RF measurements

The mechanical properties of LTCC material are relatively less good than purely ceramic materials due to the presence of glass in the LTCC composition. After the firing process, the LTCC circuit becomes denser and harder because of the burn out of the organic binder in the substrate material. This hardness makes the circuit fragile and more sensitive to mechanical

shocks. The RF characterization of LTCC circuits is normally made with a probe station, test fixture or by the use of surface mounted connectors. In each case, an important mechanical force is applied to the measured circuit which may result in damaging the circuit. Figure 2.54 shows an example of circuits broken during RF measurement using microstrip test fixture and coaxial connectors. A probe station measurement is excluded from our case due to the manufacturing limits of CPW structure in terms of line width and gap.

(a) (b)

Figure 2.54: LTCC circuit broken during RF measurements: (a) Microstrip test fixture. (b) SMP surface mount coaxial connectors

The first point that must be considered is the thickness of the fired substrate, which is essential because is resists to the normal strength created by the measurement support at the circuit. If possible, it is recommended to increase the layer count to obtain a thicker substrate, but in all cases the circuit thickness must not be less than 450 μm. In our laboratory, we developed a new measurement fixture (Figure 2.55) that is fabricated by plastic and foam material in order to decrease the mechanical load generated by the other available measurement supports. This fixture integrates coaxial connectors from SOUTHWEST MICROWAVE [19] that operate up to 40 GHz. $3D$ axis micro-positioners are also used to achieve an accurate contact between the connectors and the LTCC circuit.

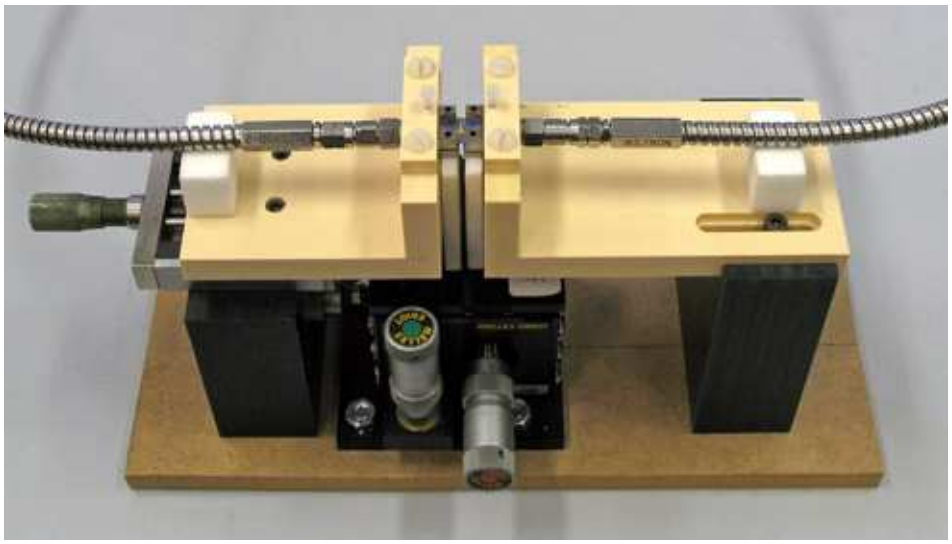


Figure 2.55: Developed fixture for RF measurement of LTCC circuits

2.5 Design rules implementation

In the previous parts of this chapter, we discussed the LTCC process validation using the available equipments in the laboratory. At the same time, we investigated the different technological problems encountered during this validation and finally we proposed suitable solutions for these problems. Initially, we started our LTCC circuit design based on the LTCC design guidelines from several LTCC circuit manufacturers (DUPONT, VTT, FERRO...). After different tests, we have been able to adapt our own DESIGN RULES that contain all dimensional values required for RF packaging design. In this section we briefly present the design guidelines implemented after LTCC manufacturing process validation.

The LTCC design guidelines make it possible for future LTCC designers at LABSTICC/TELECOM BRETAGNE to design their multilayer LTCC circuits and modules. It mentions the minimum recommended values required for design of different parts of the package (circuit dimensions, vias, lines, cavities ...). The used substrate and conductor materials from ESL are listed in the Table 2.2. Figure 2.56 shows a cross section of an LTCC package with different elements used for packaging design.

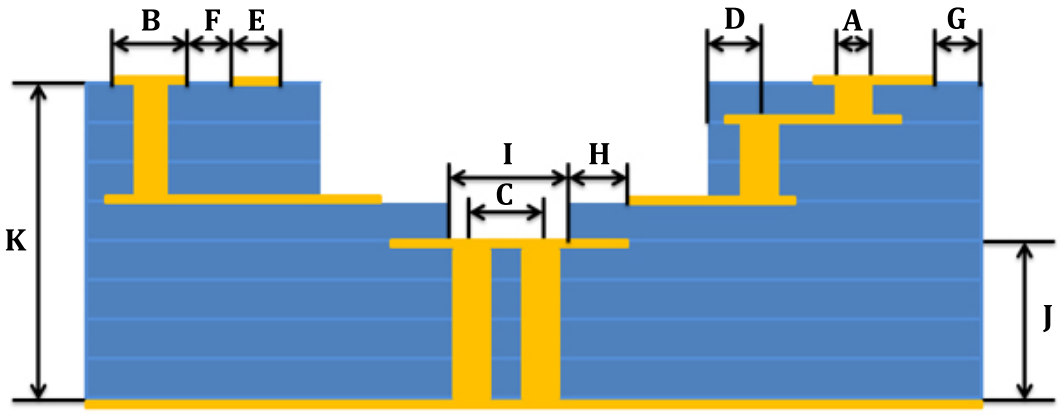


Figure 2.56: Cross section of a multilayer LTCC circuit with different elements required for package design

Referring to the figure above, the designation as well as the dimensional values of different elements are illustrated in Table 2.7. These values are expressed in the METRIC system and are given for a fired circuit.

Conclusion

In this chapter, the technological part of LTCC technology has been presented. The chapter has started by the study of different LTCC materials on the market. Due to its low permittivity value, the ESL1110 materials from ESL is selected for our applications. Next, the

Table 2.7: The minimum dimension values of different LTCC package elements

Location	Features	Dimension
A	Via diameter	150 μm
B	Via catch pad	*Via diameter* + 50 μm
C	Via spacing	3 × *via diameter*
D	Via to substrate edge	2 × *via diameter*
E	Conductor line width	105 μm
F	Conductor to conductor spacing	105 μm
G	Conductor to substrate edge	200 μm
H	Conductor to cavity edge	200 μm
I	Cavity width	1.8 mm
J	Under cavity thickness	300 μm
K	Substrate thickness	450 μm

LTCC manufacturing process validation using the available equipments in the laboratory has been discussed. The validated steps include tape preparation, via and cavity formation, via filling, screen printing, stacking, lamination and co-firing. The encountered technological problems during LTCC process validation are investigated and suitable solutions for each problem have been proposed. Finally, the DESIGN RULES required for future LTCC designers at LABSTICC/TELECOM BRETAGNE has been presented in the end of this chapter.

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Chapter 3

LTCC technology validation for RF packaging applications

Contents

Introduction

In the previous chapter, we have demonstrated that our laboratory is ready for processing multilayer circuits using the LTCC technology. This chapter describes the RF validation of this technology in order to produce microwave packages and systems in LTCC technology. This validation serves to extract ESL substrate and conductor materials properties up to 40 GHz. Section 3.1 presents some RF structures such as transmission lines and planar resonators from a theoretical point of view. In the first part (section 3.1.1), the characteristic impedance and losses of different transmission lines are studied, while the extraction method of dielectric properties (ε_r and $tan\,\delta$) from resonating structures is explained in the second part (section 3.1.2). Next, after a short presentation of circuit and EM simulators used in this thesis, section 3.2 shows simulated results of some transmission lines and microstrip resonators. Section 3.3 gives measurement results and comparison with simulations. Measurement difficulties and problems related to the LTCC circuits as well as the proposed solutions are also investigated. Next, section 3.4 shows the ESL41110 properties extraction using the free-space method up to W band. Finally, the project MM-PACKAGING that concerns the integration of MMICs in multilayer LTCC packages is presented in section 3.5.

3.1 Theoretical background

3.1.1 Transmission line theory

The choice of the right transmission line is always a great importance for any package design, because it affects the RF performance of the final package, especially at microwave and millimeter wave frequencies. A transmission line topology must be selected according to the interconnecting method at the chip and package levels. Due to its multilayer ability, the LTCC technology offers the designer a choice of transmission lines. It includes for instance microstrip, Coplanar Waveguide (CPW), Conductor Backed Coplanar Waveguide (CBCPW), and stripline. In this section we present the different planar transmission lines theory. The substrate and conductor materials selected to complete this theoretical study are the ESL41110 substrate and ESL803 gold conductor respectively (see Table 2.2).

3.1.1.1 Microstrip line

A microstrip line is normally formed by placing a strip conductor over a ground plane spaced by a supporting substrate material. Most of the E-field is located below the strip conductor. The excited mode in a microstrip line is not purely TEM; rather it is a quasi-TEM mode. This is due to that the E-field is not totally confined within the dielectric substrate and a part of this field propagates in the air surrounding the microstrip line. Figure 3.1 shows a cross section of a microstrip line with geometrical parameters needed for the design process.

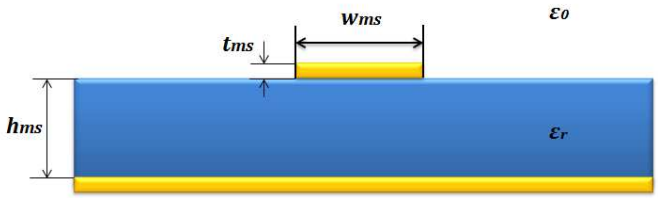


Figure 3.1: Microstrip line geometry: w_{ms} is the width of the conductor strip, h_{ms} the substrate height and t_{ms} the metalization thickness

Higher-order modes To select the substrate material, we have three principal higher-order modes that must to be considered during microstrip transmission line design. Table 3.1 summarizes these three modes:

Table 3.1: Frequency of excited surface wave modes in a microstrip line

Excited mode	Critical frequency
Dielectric mode	Equations 2.1 and 2.2
Higher-order microstrip mode	Equation 2.3
Transverse resonance mode	Equation 2.4

The critical frequencies of the expected microstrip modes for a microstrip line using the ESL41110 substrate ($\varepsilon_r = 4.2$) are shown on Figures 2.1, 2.2, 2.3 and Table 2.1. The cut-off frequencies of TM_1 (Figure 2.1 and Figure 2.2) and TE_1 (Figure 2.3) modes are plotted as a function of the substrate thickness (the thickness of one fired ESL41110 layer is about 75 μm). For our applications, the maximum operating frequency does not exceed 60 GHz. The first higher TE_1 mode appears at the seventh layer ($h = 525\ \mu m$) where the frequency is about 56 GHz. Since LTCC is a multilayer technology, this drawback can be avoided by the use of an intermediate ground plane to minimize the substrate thickness of the microstrip line. In this case, ground vias are required, which can simply be achieved using the LTCC technology.

In the same way, the transverse resonant mode frequencies are shown in Table 2.1 as a function of the substrate thickness and the strip width for a 50 Ω microstrip line impedance. This mode must be avoided by selecting a strip width as narrow as possible, which then means as few layers as possible. The substrate thickness and then the strip width can be also easily controlled with LTCC technology by using intermediate ground planes.

Microstrip impedance and loss The quasi-TEM approach leads to the definition of the effective dielectric permittivity (ε_{eff}) required for microstrip line impedance calculation. Equation 3.1 from [1] shows the analytical formulas of ε_{eff} of a microstrip line:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12\frac{h_{ms}}{w_{ms}}}} \tag{3.1}$$

where ε_r is the dielectric constant, h_{ms} is the substrate thickness and w_{ms} is the strip width.

The characteristic impedance Z_0 is thus calculated using the Equation 3.2 [1] according to the ratio $\frac{w_{ms}}{h_{ms}}$

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\varepsilon_{eff}}} ln(\frac{8h_{ms}}{w_{ms}} + \frac{w_{ms}}{4h_{ms}}) & \text{for} \quad \frac{w_{ms}}{h_{ms}} \leq 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{eff}}[\frac{w_{ms}}{h_{ms}} + 1.393 + 0.667 ln(\frac{w_{ms}}{h_{ms}} + 1.444)]} & \text{for} \quad \frac{w_{ms}}{h_{ms}} \geq 1 \end{cases} \tag{3.2}$$

Figure 3.2 represents this impedance as a function of the ratio w_{ms}/h_{ms} for some LTCC tapes with different ε_r. A 6 μm conductor thickness is used. For a 50 Ω microstrip line, the ratio w_{ms}/h_{ms} is about 2 for the ESL41110 material ($\varepsilon_r = 4.2$). Therefore, a conductor width of 150 μm is needed when using one fired ESL41110 layer ($h = 75\ \mu m$), which is easily achieved with our screen printing process.

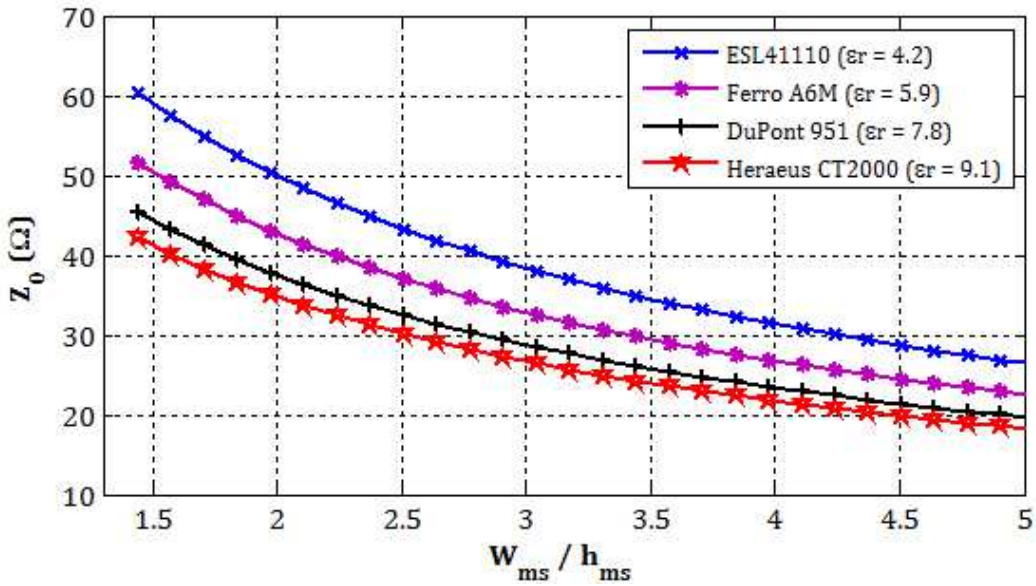


Figure 3.2: Theoretical characteristic impedance of a microstrip line as a function of the ratio strip width to substrate thickness (w_{ms}/h_{ms}). The ESL41110 material presents a ratio of 2 for 50 Ω microstrip line

The total loss in microstrip line is obtained by the sum of dielectric and conductor losses ($\alpha_T = \alpha_c + \alpha_d$) which is found in [1, 2, 3]. The conductor loss expressed in [dB/m] is calculated using the Equation 3.3 [3]:

$$\alpha_c = \frac{6.15 \times 10^{-5} A R_s Z_0 \varepsilon_{eff}}{h_{ms}} \left[\frac{w_{mse}}{h_{ms}} + \frac{0.667 \frac{w_{mse}}{h_{ms}}}{\frac{w_{mse}}{h_{ms}} + 1.444} \right] \tag{3.3}$$

where $R_s = \sqrt{\frac{\pi f \mu_0}{\sigma}}$ is the sheet resistance of the strip, $w_{mse} \approx w_{ms} + \frac{t_{ms}}{\pi}\left(1 + ln\frac{2h_{ms}}{t_{ms}}\right)$ is the effective microstrip width when the conductor thickness is taken into account, and $A = [1 + \frac{h_{ms}}{w_{mse}} + \frac{1.25}{\pi} ln\frac{2h_{ms}}{t_{ms}}]$ for $\frac{w_{ms}}{h_{ms}} \geq \frac{1}{2\pi}$.

The dielectric loss [dB/m] is calculated by the following formula:

$$\alpha_d = 8.686 \frac{k_0 \varepsilon_r \left(\varepsilon_{eff} - 1\right) tan\,\delta}{2\left(\varepsilon_r - 1\right)\sqrt{\varepsilon_{eff}}} \tag{3.4}$$

where $k_0 = \frac{2\pi f}{\lambda_0}$ is the free space wavenumber.

The conductor loss for a 50 Ω microstrip line as function of substrate thickness of ESL41110 tape is shown in Figure 3.3 (continuous lines). ESL803 gold paste is used as metallization with a conductivity of 4.1×10^7 S/m and a conductor thickness of 6 μm. The skin depth at 30 GHz for example, is about 0.42 μm which represents only 7 % of the conductor thickness, so the signal is transferred to the surface of the conductor. For this reason, the conductor loss is corrected by a roughness factor (see Equation 1.4). We see in Figure 3.3 that the conductor losses decrease as the substrate thickness increase, since the line width is also increased. But, thicker substrate can excite higher-order modes at the strip.

The LTCC material is generally a low loss substrate material. For ESL41110, the $tan\,\delta$ is in the order of 4×10^{-3}, the dielectric loss calculated from Equation 3.4 is represented in Figure 3.3 (dashed line) and does not exceed 0.25 dB/cm up to 40 GHz.

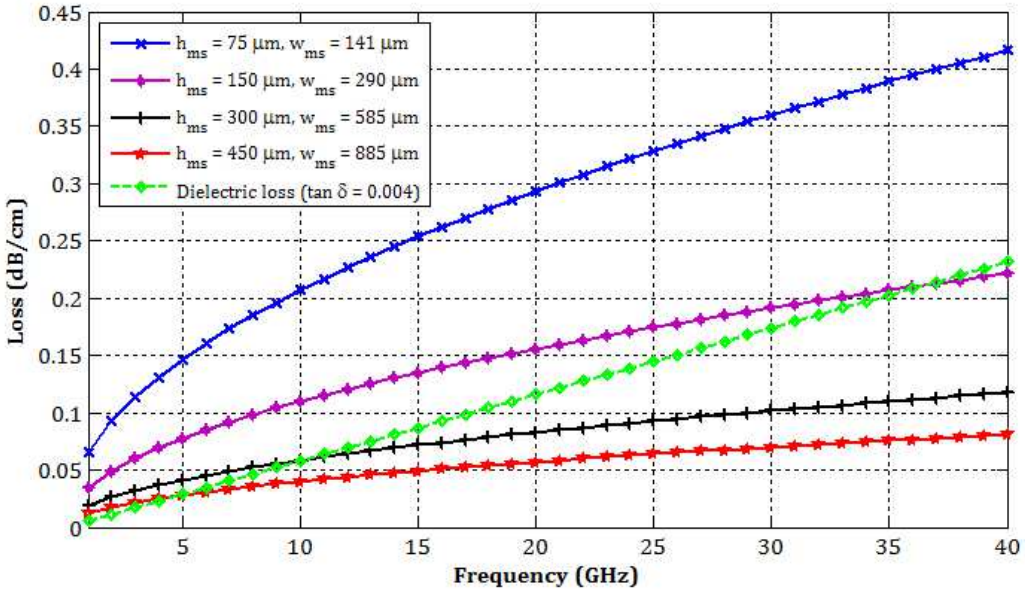


Figure 3.3: Theoretical conductor loss (continuous lines) of a 50 Ω microstrip line according to the substrate thickness of ESL41110 ($\varepsilon_r = 4.2$), $\sigma = 4.1 \times 10^7$ S/m and $t_{ms} = 6$ μm. The dielectric loss (dashed line) is calculated with $tan\,\delta = 4 \times 10^{-3}$

3.1.1.2 Coplanar waveguide line

The coplanar waveguide line is another planar transmission line which is composed of three conductor lines deposited on a substrate material. The desired coplanar mode is carried out between the central line and the external conductors representing the ground planes. If a ground plane is used below the CPW structure, it is referred to as a conductor backed coplanar waveguide (CBCPW). The CPW/CBCPW structures are a good choice for higher-frequency operation which allows better dispersion behavior than a microstrip line. It is necessary to indicate that the CPW lines are mostly used in MMIC and single layer packages while, in 3D environment such as LTCC, the CBCPW lines are more popular than CPW lines, since there is always a lower ground required for different transitions and 3D elements.

The geometry of a CPW line is represented in Figure 3.4, where w_{cpw} is the central line width, s_{cpw} is the space between the central line and the ground planes, w_{gcpw} is the ground width (in the case of finite ground CPW), and h_{cpw} is the substrate height.

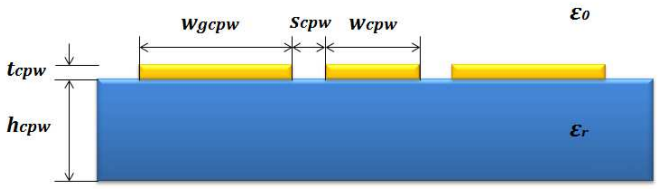


Figure 3.4: Coplanar waveguide line geometry: w_{cpw} is the width of the central conductor, s_{cpw} is the space between the central conductor and the ground plane, h_{cpw} is the substrate height, w_{gcpw} is the ground width and t_{cpw} the metalization thickness

Propagation modes Due to the symmetrical geometry of CPW structures, four modes can be excited in CPW/CBCPW lines [4]. The first one is the coplanar mode (Figure 3.5-(a)) that is excited when the E-field propagates between the central conductor and the ground planes. As in microstrip line, this mode is not a purely TEM, rather quasi-TEM because the CPW structure is not immersed in a homogeneous substrate and the conductors are in contact with the air.

The second mode excited at higher frequencies is the slot-line mode [5] (Figure 3.5-(b)). This mode usually occurs in the presence of discontinuities such as right angle bends in the structure of the line. This mode can be avoided by applying the following conditions [6]:

$$\begin{cases} w_{cpw} + 2s_{cpw} \leq \frac{\lambda_g}{10} \\ h_{cpw} > 2(w_{cpw} + 2s_{cpw}) \\ w_{gcpw} > w_{cpw} + 2s_{cpw} \end{cases} \tag{3.5}$$

where λ_g is the guided wavelength, $\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_r}}$.

The parallel plate mode is excited in the CBCPW due to the presence of bottom ground plane

(Figure 3.5-(c)). This mode can be suppressed by connecting the top and bottom ground planes with vias spaced by less than $\lambda_g/10$ [7].

Finally, the microstrip mode (Figure 3.5-(d)) is prevented in CBCPW line by ensuring that the space between the central conductor and grounds is less than the distance from the central to the lower ground plane ($s_{cpw} < h_{cpw}$) [1].

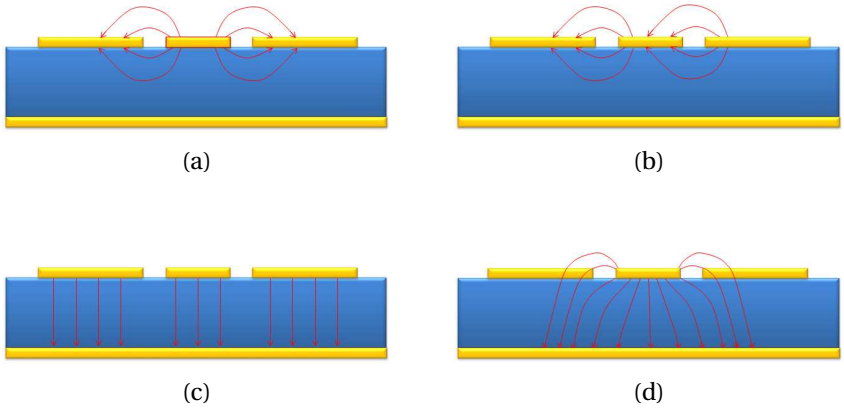


Figure 3.5: The E-fields of propagated modes on CPW/CBCPW lines: (a) The coplanar waveguide mode. (b) The slot-line mode. (c) The parallel plate mode. (d) The microstrip mode

CPW lines impedance and loss Similar to the microstrip lines, the quasi-TEM approach leads to the definition of effective relative permittivity. The analytical formulas of relative permittivity and characteristic impedance are given by Equation 3.6 and Equation 3.7 respectively. These equations are expressed in terms of the ratio of complete elliptic integral of the first kind, $K(k)/K'(k)$, where k is the variable according to the structure geometry and is different for CPW, Finite Grounded CPW (FGCPW) and CBCPW lines. The reader can refer to [8] for an interesting description of detailed mathematical calculations of various CPW structures.

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_j)}{K'(k_j)} \frac{K'(k_i)}{K(k_i)} \tag{3.6}$$

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K'(k_i)}{K(k_i)} \tag{3.7}$$

By setting $k' = \sqrt{1-k^2}$ the ratio $\frac{K(k)}{K'(k)}$ is given by:

$$\frac{K(k)}{K'(k)} = \begin{cases} \dfrac{\pi}{ln\left[2(1+\sqrt{k'})/(1-\sqrt{k'})\right]} & \text{for} \quad 0 \le k \le 0.707 \\ \dfrac{ln\left[2(1+\sqrt{k})/(1-\sqrt{k})\right]}{\pi} & \text{for} \quad 0.707 \le k \le 1 \end{cases} \tag{3.8}$$

Using the MATLAB ® software, these formulas are programmed in order to analyze the impedance of the three CPW structures on ESL41110 substrate: the infinite ground width CPW, the finite ground width CPW line and finally the conductor backed CPW lines.

In the first case, we analyze the characteristic impedance of a CPW line with infinite ground width. The two variables k_i and k_j are defined in terms of line dimensions w_{cpw}, s_{cpw}, and h_{cpw} represented on the Figure 3.4. By assuming $x = \frac{w_{cpw}}{2}$ and $y = \frac{w_{cpw}+2s_{cpw}}{2}$, the k_i and k_j are defined as follows:

$$k_i = \frac{x}{y} \tag{3.9}$$

$$k_j = \frac{sinh(\pi x/2h_{cpw})}{sinh(\pi y/2h_{cpw})} \tag{3.10}$$

Figure 3.6 plots the characteristic impedance (Z_0) according to the spacing between the central line and ground planes (s_{cpw}) and the substrate thickness (h_{cpw}) for two different central line widths (w_{cpw} = 150 and 800 μm).

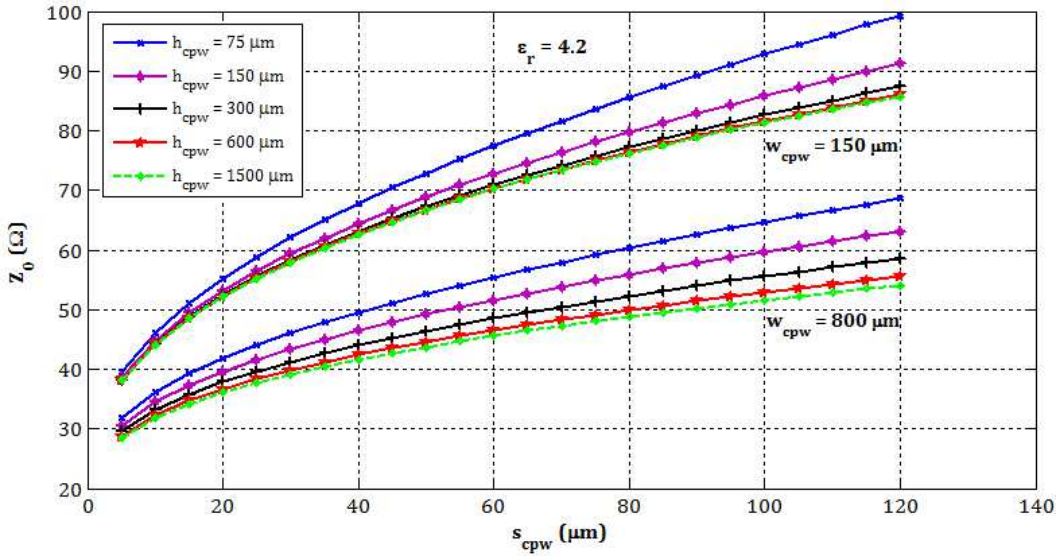


Figure 3.6: Analytical characteristic impedance values of the infinite ground CPW line as a function of space between conductors (s_{cpw}) with varying substrate thickness of ESL41110 LTCC material

As Figure 3.6 implies, the impedance Z_0 rapidly increases as the space increases for different substrate thicknesses, this is due to that the capacitive coupling decreases between the central and grounds conductors. For a 50 Ω line, the needed space on ESL41110 substrate is below 20 and 75 μm for 150 and 800 μm central conductor width respectively. On the other hand, the impedance Z_0 becomes independent of the substrate thickness as shown on the figure where Z_0 of a 600 μm (red color) thickness CPW line converges to that of a 1500 μm (green

color) thickness line. To avoid this effect, it is necessary to respect that the substrate thickness h_{cpw} does not exceed $w_{cpw} + 2s_{cpw}$. Indeed, the manufacturing of a 50 Ω CPW line on ESL41110 substrate is impossible in our laboratory, because the screen printing width and space dimensions are limited to be larger than 100 μm.

Next, to verify the effect of the ground width on the line impedance, we treated the impedance Z_0 of finite ground width CPW line. Equations 3.6 and 3.7 are still valid for this calculation and the new k_i and k_j expressions [8] are used instead the previous ones:

$$k_i = \frac{x}{y}\sqrt{\frac{1-y^2/z^2}{1-x^2/z^2}} \tag{3.11}$$

$$k_j = \frac{sinh(\pi x/2h_{cpw})}{sinh(\pi y/2h_{cpw})}\sqrt{\left(1-\frac{sinh^2(\pi y/2h_{cpw})}{sinh^2(\pi z/2h_{cpw})}\right)/\left(1-\frac{sinh^2(\pi x/2h_{cpw})}{sinh^2(\pi z/2h_{cpw})}\right)} \tag{3.12}$$

where x and y are the same variables used in infinite CPW line and $z = w_{gcpw} + y$, with w_{gcpw} the top coplanar ground width.

Figure 3.7 shows the analytical characteristic impedance (Z_0) as a function of the ground width (w_{gcpw}) for varying space s_{cpw}. The substrate thickness corresponds to eight ESL41110 layers (600 μm) and the central line width is 800 μm. From this figure, taking as an example the space s_{cpw} of 75 μm, when the ground width is reduced, Z_0 tends to increase slightly. This is related to the decreased coupling between conductors. In addition, if the space s_{cpw} increases, the line impedance increases and thus the 50 Ω CPW line is still not feasible even when varying the ground width.

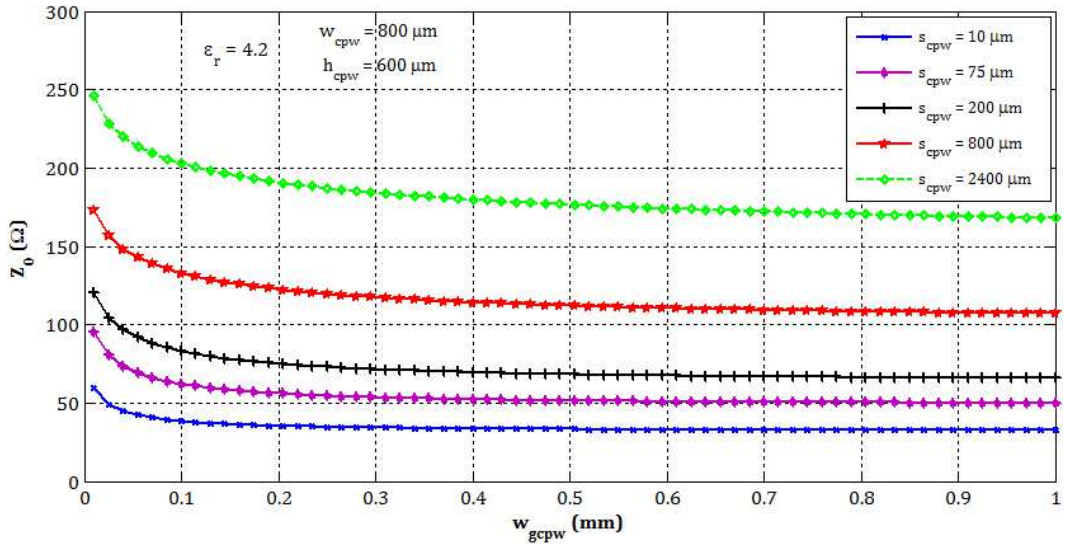


Figure 3.7: Characteristic impedance of FGCPW lines on ESL41110 substrate as a function of ground width w_{gcpw} and varying space width s_{cpw}

In conclusion, CPW lines are excluded in our case due to the fabrication process limitations.

After this analyze, we will now treat the CBCPW line. This configuration is required for vertical transitions to microstrip and stripline where a bottom ground plane is needed. The effective permettivity and the characteristic impedance are defined by the following equations [8]:

$$\varepsilon_{eff} = 1 + (\varepsilon_r - 1)\frac{K(k_j)/K'(k_j)}{K(k_i)/K'(k_i) + K(k_j)/K'(k_j)} \tag{3.13}$$

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}}\frac{1}{K(k_i)/K'(k_i) + K(k_j)/K'(k_j)} \tag{3.14}$$

where $K(k)/K'(k)$ is the elliptic integral of the first kind, and the variables k_i and k_j are expressed in terms of the line dimensions.

$$k_i = \frac{x}{y} \tag{3.15}$$

$$k_j = \frac{tanh(\pi x/2h_{cpw})}{tanh(\pi y/2h_{cpw})} \tag{3.16}$$

The CBCPW geometry is the same as a CPW line except that a ground plane is added at the bottom substrate surface (Figure 3.5). The characteristic impedance Z_0 of CBCPW lines is plotted in the following figure:

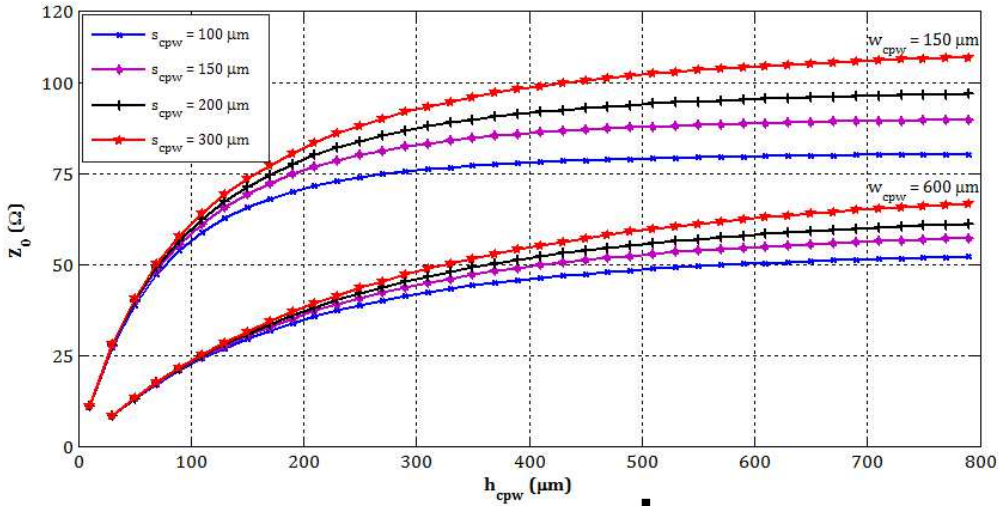


Figure 3.8: Characteristic impedance of CBCPW line on ESL41110 material as a function of substrate thickness with varying strip and space widths

As represented in Figure 3.8, Z_0 increases according to the substrate thickness for the two

strip widths (w_{cpw} = 150 and 600 μm) and for the space varied between 100 and 300 μm. For narrow lines such as 150 μm conductor width, the impedance at Z_0 = 50 Ω is unchanged for different spaces. For the wide conductor, the CPW mode appears and the impedance Z_0 vary with the substrate thickness. In addition, the characteristic impedance decreases when compared to a CPW line since a stronger capacitive coupling is generated between the central conductor and the lateral ground as well as between the central conductor and backed conductor.

Finally, the CBCPW configuration is the better choice for our LTCC substrate, because the impedance can be controlled by a reasonable space width (larger than 100 μm), that is simply realized by screen printing. Due to the back ground plane, the CBCPW structure is more suitable for a 3D environment where a ground plane is needed for different transitions. In order to suppress the parallel plate mode, it is important to connect the two ground planes by metalized vias which can easily be achieved in LTCC technology.

Now, we analyze the conductor and dielectric losses of the CBCPW line, which we intend to use with ESL41110 substrate. Normally, conductor loss in a CPW structure is computed using formulas found in [3], with air above the transmission line. Yet other formulas exist, as the ones treated by GHIONE in [9] which are used in the AGILENT product LINECALC. Figure 3.9 shows the conductor loss of a 50 Ω CBCPW line calculated by LINECALC for different substrate thicknesses. The dielectric losses are not taken into account since $tan\,\delta$ is set to 0, the metal conductivity is 4.1×10^7 (S/m) and the conductor thickness is 6 μm. As the figure illustrates, losses decrease when the substrate thickness increases.

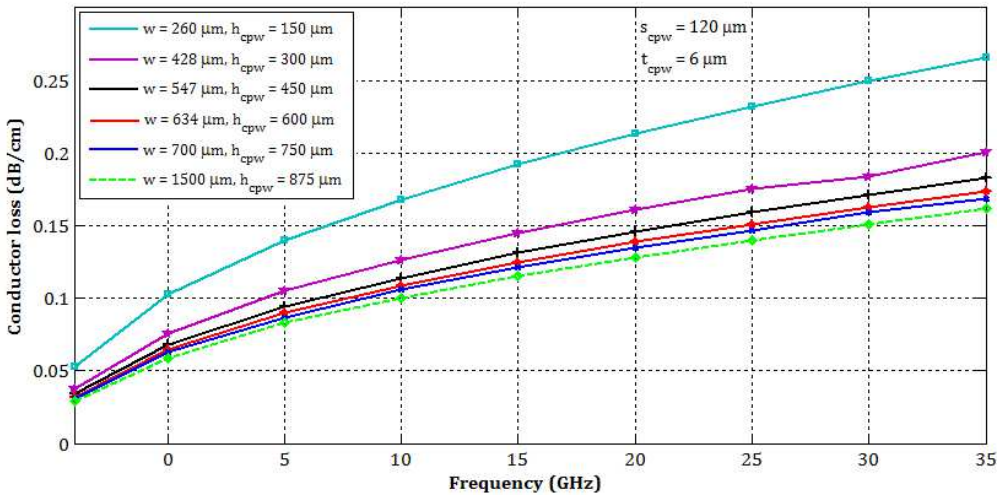


Figure 3.9: Conductor loss of 50 Ω CBCPW line in ESL41110 tape according to the substrate thickness

In the same manner, the conductor losses are analyzed by varying the space of the central strip to grounds (Figure 3.10). The conductor losses increase when the space between conductors decreases. This is due - in the two cases (varying h_{cpw} and s_{cpw}) - to an increased capacitive coupling between the central line and ground planes. In order to minimize the attenuation

due to the conductor losses, it is necessary to keep the substrate thickness and central strip to ground spacing as large as possible, but it must be carefully done in order to avoid excitation of higher-order modes.

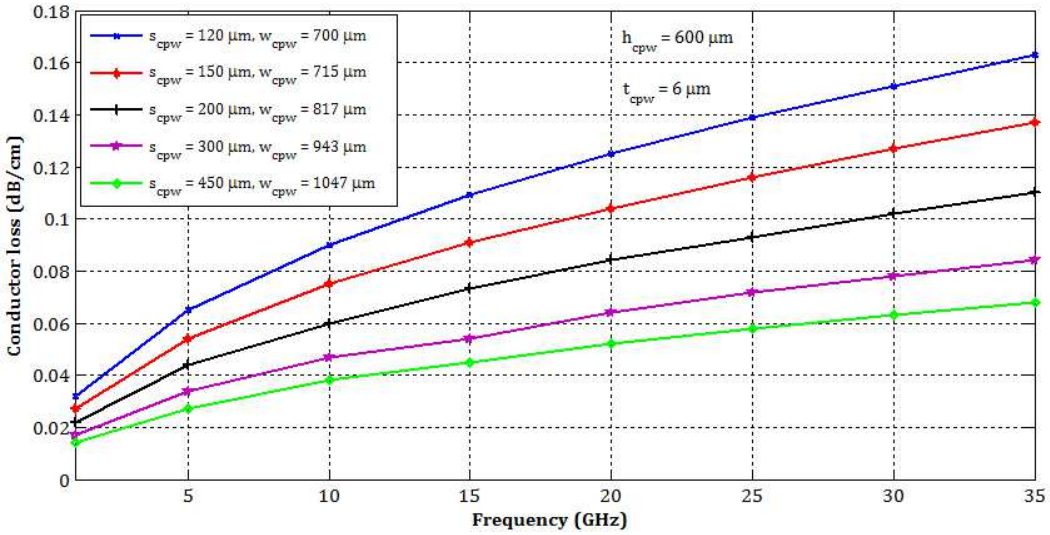


Figure 3.10: Conductor losses of a 50 Ω CBCPW line in ESL41110 substrate with varying spacing of the center conductor to top ground planes

The attenuation due to dielectric losses can be calculated using the same formula as for the microstrip line (Equation 3.4). In the same way, the dielectric loss for CBCPW line is also computed by LINECALC, the loss tangent of ESL41110 material is 0.004 and the metal is a perfect conductor. The calculated dielectric losses are about $0.2 dB/cm$ at 40 GHz.

3.1.1.3 Stripline

Stripline, also referred to as a triplate line, is formed by placing a conductor between two parallel ground planes. The stripline surrounding is filled with a uniform dielectric substrate creating a pure TEM mode. The main benefits of stripline are that no dispersion occurs as in microstrip or CPW structures, and it presents excellent electrical isolation when compared to the other transmission lines. But, it is difficult to access to the signal because it is embedded inside the substrate, and this requires the design of specific transitions. to build transitions. The stripline geometry is shown in the Figure 3.11:

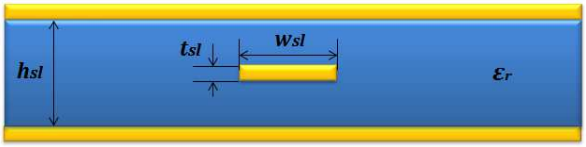


Figure 3.11: Stripline geometry: w_{sl} is the conductor width, h_{sl} the substrate height and t_{sl} the metalization thickness

Stripline modes The fundamental excited mode in a stripline is the TEM mode. Higher order parallel plate modes (TE and TM modes) can be excited due to the presence of the parallel ground planes. These modes can be avoided by shorting the two ground planes using metalized vias, and by keeping the substrate thickness h_{sl} less than $\lambda_g/4$ [1]. Thus, the cut-off frequency for both TE_1 and TM_1 mode is given by Equation 3.17:

$$f_c = \frac{c}{2h_{sl}\sqrt{\varepsilon_r}} \tag{3.17}$$

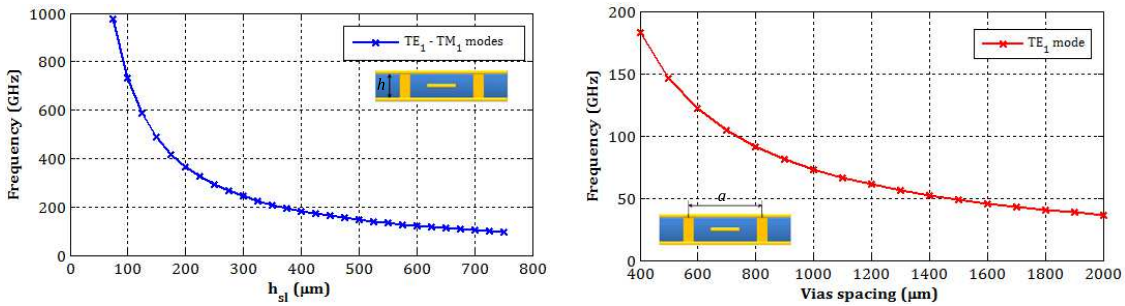
where c is the free-space velocity, h_{sl} the parallel plate distance and ε_r the the relative permittivity of the substrate.

On the other hand, with shielding vertical vias on the side walls, a stripline structure is represented as a rectangular waveguide with cut-off frequency of the first propagating mode TE_{10} as shown in Equation 3.18:

$$f_c = \frac{c}{2a\sqrt{\varepsilon_r}} \tag{3.18}$$

where a is the distance between the shielding vias placed between the stripline.

The next figures show the cut-off frequency of the higher mode excited in a stripline for the ESL41110 ($\varepsilon = 4.2$) substrate material as functions of the substrate thickness (for parallel plate mode) and the metalized vias spacing (for waveguide mode). This frequency decreases when the substrate thickness and vias pitch increases. For example, the excited TE_1 and TM_1 modes have a 100 GHz cut-off frequency for substrate thickness of 750 μm (10 layers), while the waveguide TE_{01} mode appears at about 70 GHz when the via spacing exceeds 1 mm.



(a) (b)

Figure 3.12: Higher-order mode frequencies excited in a stripline embedded inside ESL substrate: (a) Cut-off frequency of parallel plate mode according to the ground spacing. (b) Cut-off frequency of waveguide mode as function of shielding via spacing

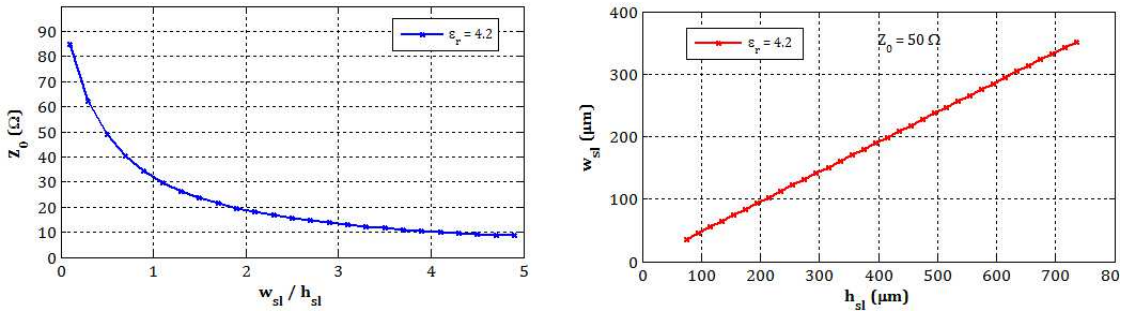
Stripline impedance and losses The characteristic impedance (Z_0) of a stripline is calculated according to the stripline width (w_{sl}), the ground planes distance (h_{sl}) and the dielectric constant (ε_r). An approximate expression for the characteristic impedance of a stripline, with zero-thickness strip, is given by Equation 3.19 [1]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{1}{\frac{w_{esl}}{h_{sl}} + 0.441} \tag{3.19}$$

where w_{esl} is the effective width of the central conductor given by:

$$\frac{w_{esl}}{h_{sl}} = \frac{w_{sl}}{h_{sl}} - \begin{cases} 0 & \text{for} \quad \frac{w_{sl}}{h_{sl}} < 0.35 \\ (0.35 - \frac{w_{sl}}{h_{sl}})^2 & \text{for} \quad \frac{w_{sl}}{h_{sl}} < 0.35 \end{cases} \tag{3.20}$$

Figure 3.13-(a) shows the characteristic impedance of a stripline embedded in the ESL41110 substrate as a function of the $\frac{w_{sl}}{h_{sl}}$ ratio. The characteristic impedance decreases as $\frac{w_{sl}}{h_{sl}}$ increases. For a 50 Ω line, this ratio is about 0.47. Figure 3.13-(b) illustrates the central conductor width according to the parallel plate spacing, the layer count must be equal to or greater than 4 to obtain a conductor greater than 120 μm width in order to avoid screen printing problems.



(a) (b)

Figure 3.13: Characteristic impedance of stripline with ESL41110 substrate: (a) The impedance variation as function of $\frac{w_{sl}}{h_{sl}}$ ratio. (b) Central conductor width according to the grounds spacing for a 50 Ω stripline

The attenuation due to the conductor losses in a stripline can be found using WHEELER'S INCREMENTAL INDUCTANCE RULE method and is approximated in [Np/m] as by the following expressions [1]:

$$\alpha_c = \begin{cases} \frac{2.7\times10^{-3} R_s \varepsilon_r Z_0}{30\pi(h_{sl}-t_{sl})} A & \text{for} \quad \sqrt{\varepsilon_r} Z_0 < 120 \\ \frac{0.16 Rs}{Z_0 h_{sl}} B & \text{for} \quad \sqrt{\varepsilon_r} Z_0 > 120 \end{cases} \tag{3.21}$$

where R_s is the sheet resistance of the central conductor, and A and B expressions are defined as follows:

$$A = 1 + \frac{2w_{sl}}{h_{sl}-t_{sl}} + \frac{1}{\pi}\frac{h_{sl}+t_{sl}}{h_{sl}-t_{sl}} ln(\frac{2h_{sl}-t_{sl}}{t_{sl}})$$

$$B = 1 + \frac{h_{sl}}{(0.5w_{sl}+0.7t_{sl})}(0.5 + \frac{0.414t_{sl}}{w_{sl}} + \frac{1}{2\pi} ln\frac{4\pi w_{sl}}{t_{sl}})$$

Figure 3.14 shows the conductor loss behavior according to the frequency for a 50 Ω stripline using the ESL41110 substrate. The losses decrease in the case of larger ground plane spacing or rather larger conductor width.

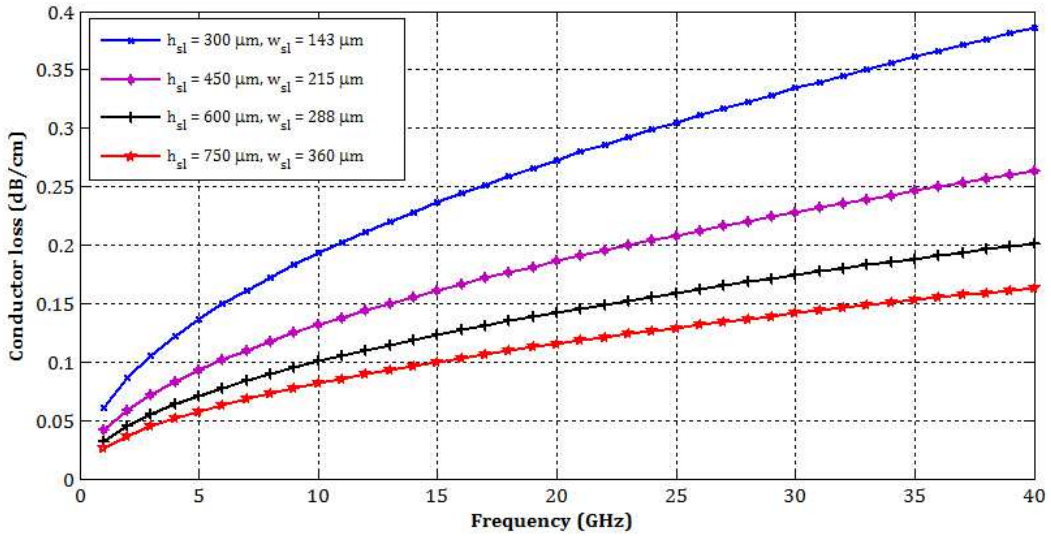


Figure 3.14: Conductor losses of a 50 ohm stripline for different ESL41110 substrate height

Dielectric loss in stripline is higher than that of microstrip or CPW lines, due to the fact that all the E-field is located inside the dielectric substrate. The attenuation due to dielectric loss in [Np/m] has the same expression as TEM lines and is given by Equation 3.22:

$$\alpha_d = \frac{k}{2} tan\,\delta \tag{3.22}$$

where k is the wavenumber in the dielectric and $tan\,\delta$ is the loss factor of the substrate material. The calculated dielectric loss of a stripline in the ESL41110 substrate ($tan\,\delta = 0.004$) is about 0.3 dB/cm at 40 GHz.

3.1.2 Planar microstrip resonators theory

When designing an RF package (especially at higher frequencies), it is necessary to know the precise values of the dielectric constant and loss tangent of the material. The reason is to

obtain precise circuit dimensions that are very sensitive at high frequencies. Several methods based on planar resonators, waveguide resonators and quasi-optical approach are used to extract the dielectric material properties.

The planar resonator method is the most preferred over the other methods due to its simplicity, but the extraction is limited to set of single frequencies (at resonant frequencies) while the values can be interpolated between these frequencies. An estimation of the dielectric constant and the dissipation factor is necessary over a large frequency band. This section gives a theoretical background on planar resonating structures employing ring and T-junction resonators.

3.1.2.1 Ring resonator

The microstrip ring resonator shown in Figure 3.15 consists of a closed loop ring placed between two transmission lines with two coupling gaps between the ring and the microstrip lines. The advantage of ring resonator over the half wavelength resonator is that it has no open-end effects and thus it is free of radiating losses [8]. The size of the coupling gaps should be adjusted in order to obtain strong coupling between the microstrip line and the ring.

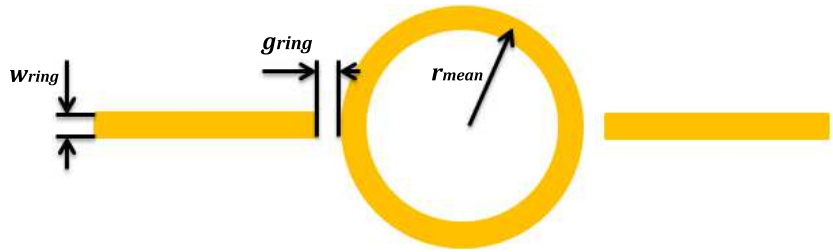


Figure 3.15: Geometry of a microstrip ring resonator: w_{ring} is the microstrip width, g_{ring} is the coupling gap and r_{mean} is the mean ring radius

Equation 3.23, from [10], shows that the multiple guided wavelengths in the ring resonator is equal to the mean circumference of the ring:

$$n\lambda_g = 2\pi r_{mean}\,, \quad n = 1,2,3... \tag{3.23}$$

where n is the mode number, λ_g is the guided wavelength and r_{mean} is the mean radius of the ring.

The effective permittivity is defined as the square of the ratio of the speed of light in free space to the phase velocity ($\frac{1}{f\lambda_g}$) in a microstrip line:

$$\varepsilon_{eff}(f) = \left(\frac{c}{f\lambda_g}\right)^2 \tag{3.24}$$

Replacing Equation 3.23 in Equation 3.24, the effective permittivity of the substrate material at the resonant frequency f_n is evaluated by the following Equation [10]:

$$\varepsilon_{eff}(f_n) = \left(\frac{nc}{f_n 2\pi r_{mean}}\right)^2 \tag{3.25}$$

As shown in Figure 3.16, the loaded Q factor (Q_L) of a ring resonator is obtained by the measurement of the transmission coefficient (S_{21}) at the resonant frequency by $Q_L = \frac{f_0}{f_2 - f_1}$.

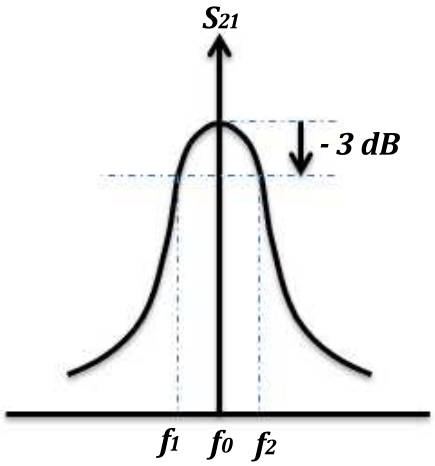


Figure 3.16: The loaded Q factor measurement of ring resonator

Equation 3.26 shows the unloaded Quality factor (Q_u) of the ring resonator which is calculated as a function of the loaded quality factor Q_L and the transmission coefficient S_{21} (in linear scale) at the n^{th} resonant frequency [11]:

$$Q_u = \frac{Q_L}{1 - S_{21}(n)} \tag{3.26}$$

The total attenuation in [Np/m] of the ring resonator is calculated by Equation 3.27 [11]. This includes the attenuation due to the conductor, dielectric, radiation and surface wave losses. The radiation and surface wave losses are normally neglected.

$$\alpha_{tot} = \frac{n\pi}{Q_u L_{res}} = \frac{n\pi}{Q_u 2\pi r_{mean}} \tag{3.27}$$

Finally, the dielectric constant at the corresponding resonant frequency is extracted using Equation 3.1. Similarly, the conductor and dielectric losses are calculated using Equation 3.3 and Equation 3.4 respectively. The loss tangent is normally deduced from this last equation. It is necessary to take into account the surface roughness of LTCC material in the conductor loss computation.

3.1.2.2 T-junction resonator

The microstrip T resonator is another technique used to extract the dielectric material using the insertion loss measurement (from S_{21} parameter) of a microstrip transmission line loaded with an open stub as shown in Figure 3.17. The resonant frequency is varied according to the stub length. The main drawback of the T-junction resonator is that it has an open end, which requires to take into account the radiation losses in the design.

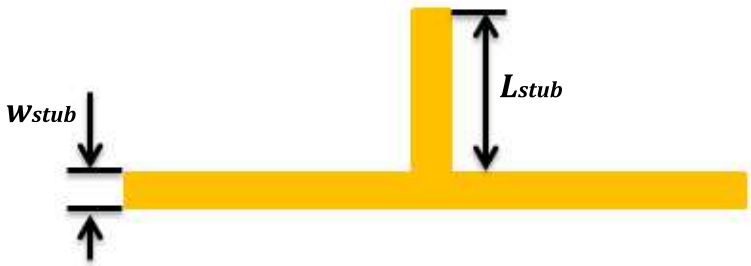


Figure 3.17: The microstrip T resonator geometry

The resonant frequency of the T-junction circuit is expressed according to the stub length by Equation 3.28:

$$(2n+1)\lambda_g = 4L_{stub} \tag{3.28}$$

The principle of parameter extraction is the same as the ring resonator. The equations used above for loaded and unloaded Q factors as well as the total attenuation remain valid for the microstrip T-junction resonator. The effective permittivity is calculated from Equation 3.29 which is expressed according to the stub length [12]:

$$\varepsilon_{eff}(f) = \left(\frac{nc}{4L_{stub}f}\right)^2, \quad n = 1,3,5... \tag{3.29}$$

3.2 LTCC circuit simulations

After the theoretical discussion in the previous section (section 3.1.1), we present here the simulation results of some designed transmission lines (microstrip and CBCPW lines) and microstrip planar resonators (ring and T-junction) using the ESL41110 substrate material. We also give a short introduction to the circuits and electromagnetic simulators used in this thesis.

3.2.1 Circuit and EM simulations

The CAD design process has been presented in section 2.2 in term of layout processing required for LTCC circuit manufacturing. A part of this CAD design is dedicated to the circuit design in terms of electrical schematic simulation and EM modeling in order to predict the performance of RF LTCC structures. Circuit simulations are achieved in this thesis using ADS® product from AGILENT TECHNOLOGIES [13], while 3D EM simulations are conducted with HIGH FREQUENCY STRUCTURE SIMULATOR (HFSS®) from ANSOFT [14], and in some cases with MOMENTUM, from AGILENT, for 2.5D EM simulations.

3.2.1.1 Circuit simulations

The circuit simulation of RF structures is used largely today. It allows the design of RF devices by combining analytical models or electrical equivalent schematic of basic components. These components can be active or passive and simulation types can be linear or non-linear, in the frequency or time domain. For instance, the design of active devices such as MMIC chips can quasi-exclusively be realized thanks to ADS® software and the passive devices (localized and distributed) can be performed in ADS® or ANSOFT DESIGNER® softwares.

The chip environment (package and interconnections) can be partially taken into account in the MMIC circuit simulation by analytical models of transitions or interconnections. For example, when a MMIC chip is connected by a wire bonding, the wire is usually represented by equivalent inductances, which is an approximation of the main effect. But in the case of complex geometries as in LTCC packages where vertical transitions and 3D interconnections are required, the analytical models are quickly obsolete and do not cover the EM coupling effect that is the main characteristic of LTCC package. In this case, a 3D EM simulation is required in order to obtain an accurate RF performance of LTCC structures.

Circuit simulations in this thesis are conducted with ADS® software that consists of a suite of software's allowing the study of microwave circuits, whether linear or not. It is normally divided into two parts:

- Digital Signal Processing (DSP): ADS® allows the system simulation of various communication systems (analog/digital). For example, system modeling of a complete transceiver chain can be achieved.

- RF Design: the circuit simulator uses analytical models for passive (transmission lines, discontinuities...) and active (diodes, transistors...) circuits. The RF design in ADS® gives access to a 2.5*D* EM simulator MOMENTUM® using the method of moments.

Finally, as our goal is to characterize LTCC technology for RF packaging applications, ADS® circuit simulation type used in this thesis includes only linear simulations using S-parameters.

3.2.1.2 EM Simulation

EM simulation resolves MAXWELL'S equations defining the laws of electromagnetism thanks to numerical methods. The wave propagation in a structure for a given geometry and materials is calculated, and thus allows the EM characterization of this structure.

There are several EM simulation methods, where MAXWELL'S equations are treated in different mathematical forms and boundary conditions. For example, in the method of moment (MoM), MAXWELL'S equations are resolved using the integral equations form while, in the Finite Difference Time Domain (FDTD) method, these equations are resolved in the form of differential equations. These methods can be in the frequency domain (MoM, Finite Element Method (FEM)...) or in the time domain (FDTD, Transmission Line Matrix (TLM)...) and adapted to 2.5D and 3D geometry problems.

To apply these methods to RF package geometries, EM simulators must imperatively be able to support 3D problems. However, the EM simulation includes only the passive structures in order to reduce the simulation complexity and the EM coupling between the active element and the package is neglected. Thus, the design of microwave packages integrating active circuits is today made separately with EM simulation of package and circuit simulation of active component alone. As in ADS®, the effect of the package on the active circuit performance can be analyzed by combining both circuit and EM simulations.

HFSS® software is one of the 3D full EM simulator universally used for RF characterization of different 3D geometry structures. This one uses finite element method in the frequency domain to solve MAXWELL'S equations and generate S-parameters in some medium characterized by its dielectric, magnetic and conductive materials. The starting point is to mesh the studied volume into a number of elementary cells (the finite elements): the E and H fields are evaluated at these cells normally under tetrahedral and triangular forms for the volume and surface geometry respectively. HFSS® simulator supports different types of boundary conditions (perfect conductor, radiation, surface impedance...) and wave and lumped ports can be used for structure characterization in terms of S, Y or Z parameters. Finally, there are three types of analysis in HFSS®. The first is a discrete analysis where the calculation is done entirely at each chosen discrete frequency. This method is more accurate but requires more computation time especially for large frequency bands. Other type are based on extrapolation algorithms, the calculation is performed at a given frequency, called the center frequency. Then the solution is extrapolated thanks to an algorithm on the entire frequency band. This analysis called interpolating saves computing time but, the extrapolation is not precise on broadband frequency, especially when high accuracy is desired. The third type that called fast sweep is recommended for resonating structures with narrow frequency band while interpolate analysis allows greater precision over a wide frequency band (max 20 GHz) but it is not adapted for resonating structures.

MOMENTUM is a 2.5D EM simulator that uses the method of moments (MoM) to solve MAXWELL equations in the frequency domain. MOMENTUM is more used for planar circuits

and MMIC analysis and modeling. It allows multilayer circuit, but, as it forces the dielectric levels to extend to infinity in al1 directions, is not always applicable to complex 3D geometry such as LTCC transitions. EM simulations conducted in this thesis using MOMENTUM are rather planar transmission lines and resonators structures at one level.

3.2.2 Transmission line simulations

The basic element of an RF package or module is the transmission line. It is usually used to interconnect any component (active or passive) or transition in order to input and output RF signals on the MMIC chip. In this section, we present the design and simulation results of several transmission lines (in microstrip and CBCPW topology) needed for packaging applications in LTCC technology up to 40 GHz.

Several papers discuss transmission lines and feedthroughs in LTCC technology [15, 16, 17]. Beyond the material properties (substrate and conductor), the design of transmission lines plays an important role on the RF performance of the package. The proposed structures in this section which are designed to be free resonance and low loss transmission lines, are examined in ADS® and HFSS® softwares with the respect of the design rules of the LTCC technology developed in our laboratory (section 2.5).

The first step is to make simulations for simple planar transmission lines that contain microstrip and CBCPW lines. The CPW line is excluded from this study due to the manufacturing difficulties in term of screen printing process. The substrate material is ESL41110 with a dielectric constant of 4.2 and a dissipation factor of 0.004 at 1 GHz while the ESL803 gold paste ($\sigma = 4.1 \times 10^7 S/m$) is used as metalization.

3.2.2.1 Microstrip

The two 50 Ω microstrip lines (12.5 mm length) examined in this section are originally designed using ADS® software up to 40 GHz. The first line is implemented on six ESL41110 layers, while the second is analyzed in eight LTCC layers with an added intermediate ground plane plane at the sixth layer. The LTCC layer thickness is 75 μm after firing and the conductor thickness is about 6 μm. We note that vertical ground vias are used in the second line in order to connect the lower and the intermediate ground planes. The via diameter is 160 μm and via spacing from center to center is about 450 μm. The Table 3.2 shows the dimensions of the two microstrip lines.

Table 3.2: 50 Ω microstrip line geometry

Parameter	Line 1	Line 2
Layer count	6	8
h_{ms}	450 μm	150 μm
w_{ms}	880 μm	290 μm

Figure 3.18 shows the E-fields at 20 GHz and simulation results in term of S-parameters for the two microstrip lines. The half of the structures is simulated with HFSS® software using a symmetry boundary in order to reduce the simulation time.

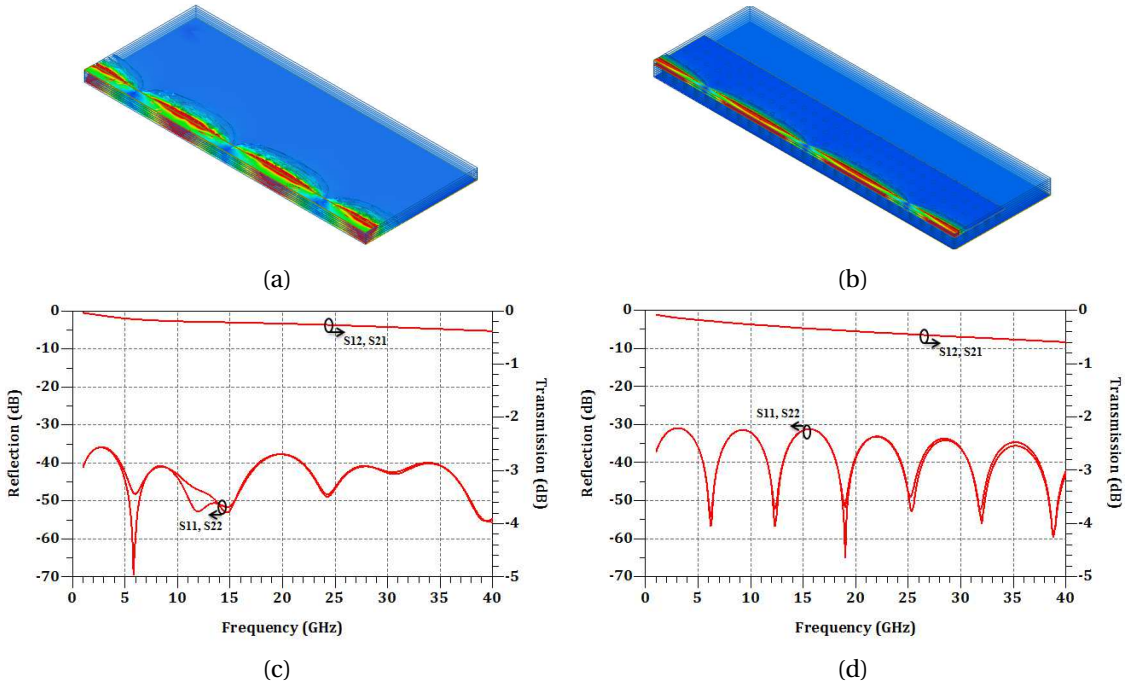


Figure 3.18: HFSS simulation of two 50 Ω microstrip lines: (a) E-field at 20 GHz in microstrip line of "Line 1" on six ESL41110 layers. (b) E-field in microstrip line of "Line 2" on eight ESL41110 layers with intermediate ground plane. (c) S-parameter results of "Line 1". (d) S-parameter results of "Line 2"

As this figure shows, the return loss of the two lines is better than 30 dB between 1 and 40 GHz. The insertion loss does not exceed 0.5 dB at 40 GHz. By simple comparison to the theoretical losses represented in Figure 3.3, the conductor loss values for the two microstrip lines "Line 1" and "Line 2" is 0.07 dB/cm and 0.22 dB/cm, while the dielectric loss is about 0.23 dB/cm at 40 GHz. Taking into account the microstrip line length of 12.5 mm, the total theoretical losses at 40 GHz is about 0.317 dB (Line 1) and 0.505 dB (Line 2) which is very close to the values represented in Figure 3.18 ((c) and (d)).

3.2.2.2 Conductor backed coplanar waveguide

After microstrip line simulation, the next step concerns the simulation of CBCPW line using LTCC substrate. Table 3.3 shows the dimensions of a designed 50 Ω CBCPW in eight ESL41110 layers. The ESL803 gold conductor with conductivity of 4.1×10^7 S/m is used as metalization. The conductor thickness is 6 μm. In order to avoid parallel plate and waveguide modes between ground planes, ground vias are used to interconnect the lower and the top ground planes.

Simulation of the CBCPW line is made using HFSS® up to 20 GHz. Figure 3.19 illustrates the

Table 3.3: 50 Ω CBCPW line dimensions

Parameter	Dimension
w_{cpw}	600 μm
s_{cpw}	120 μm
h_{cpw}	600 μm
L_{cpw}	8.5 mm
Via diameter	220 μm
Via spacing	750 μm

simulation results of S-parameter that shows a return loss and transmission loss better than 30 dB and 0.2 dB between 1 and 20 GHz respectively.

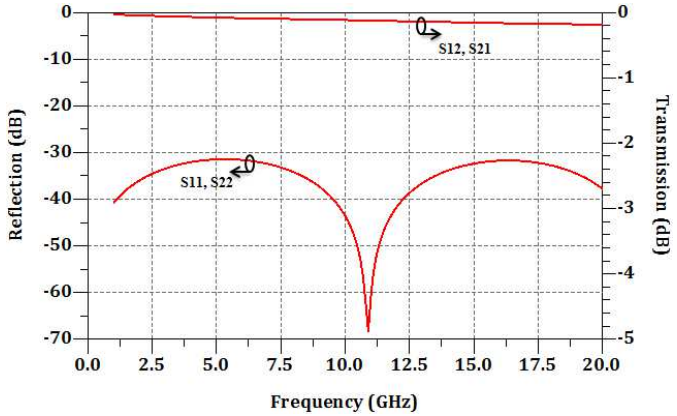


Figure 3.19: S-parameter results of simulated CBCPW line using eight ESL41110 layers

Similarly, the theoretical conductor loss of the CPCPW line is about 0.14 dB/cm at 20 GHz (see Figure 3.9) while the dielectric loss is 0.08 dB. The total loss of 8.5 mm CBCPW line is 0.205 dB which is close to the simulated transmission loss represented on the Figure 3.19 (at 20 GHz)

3.2.3 Microstrip resonator simulations

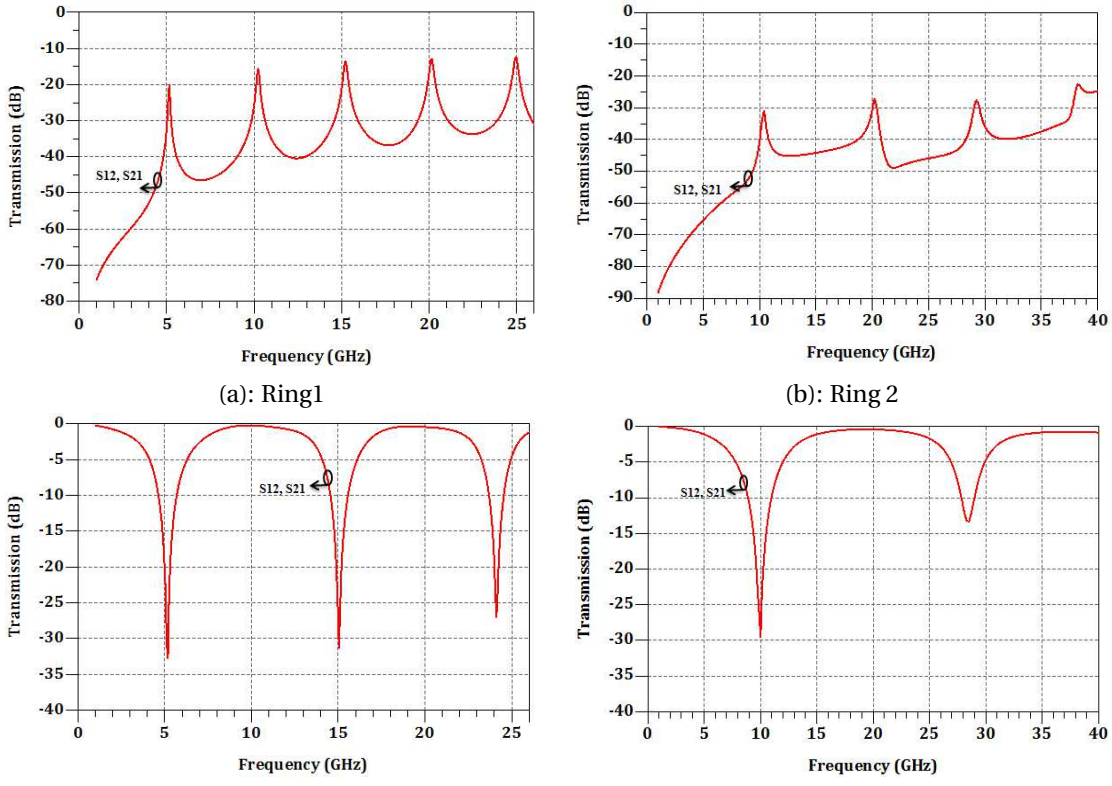
The four resonators (two rings and two T-junctions) presented in this section are implemented on six ESL41110 LTCC layers. The resonators named "Ring 1" and "T1" are simulated up to 26 GHz and are designed to be measured using surface mount SMP connectors [18]. The others named "Ring 2" and "T2" are simulated up to 40 GHz for measurement in the microstrip test fixture. The substrate thickness of six ESL41110 layers is 450 μm (the thickness of one fired layers is 75 μm). Assuming a dielectric constant of 4.2 and loss tangent of 0.004, the microstrip line width is 880 μm for 50 Ω characteristic impedance. Table 3.4 show dimensions of the designed resonators.

Initially the resonant frequencies of ring and T-junction are calculated by Equation 3.23 and

Table 3.4: Planar microstrip resonators geometry

Parameter	Ring 1	Ring 2
r_{mean}	5 mm	2.6 mm
L_{ring}	31.5 mm	16.335 mm
g_{ring}	120 μm	450 μm
	T1	**T2**
L_{stub}	8 mm	4 mm

Equation 3.28 respectively according to the mean radius and T-junction length. Then, ADS® software is first used to simulate these resonators and finally, in order to obtain accurate results, the resonators are simulated using HFSS® software. Figure 3.20 shows the simulated transmission factor of the four resonators "Ring 1", "Ring 2", "T1" and "T2".



(a): Ring1 (b): Ring 2

(c): T1 (d): T2

Figure 3.20: HFSS® simulation of transmission factor of planar microstrip resonators on six ESL41110 layers

3.3 LTCC circuit fabrication and measurement

The simulated transmission lines and resonators presented above are fabricated using the LTCC manufacturing process discussed in section 2.3. Several prototypes which include trans-

mission lines and resonators are fabricated according to the chosen measurement method. Some circuits include surface mount SMP [18] and MINI-SMP [19] connectors, while others are designed to be measured in microstrip test fixture. Figure 3.21 shows some realized circuits for microstrip lines and resonators. These circuits were not completely tested in terms of S-parameters due to the circuit fragility, poor edge quality after cutting them into parts (see section 2.4.7). To avoid these problems, we have proposed, as discussed in section 2.4.8, a solution for measurement of LTCC circuits which concern the use of the developed test fixture shown in Figure 2.55.

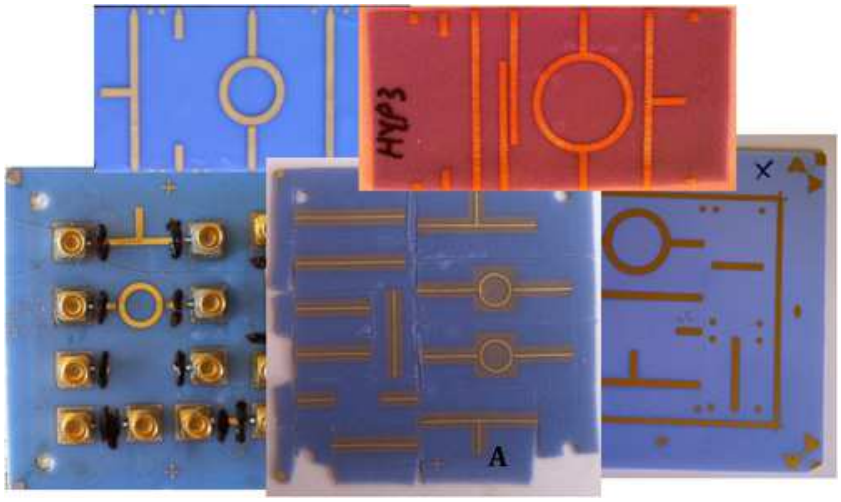


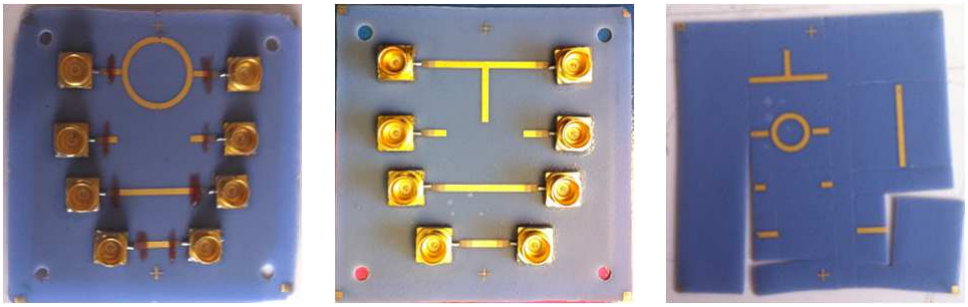
Figure 3.21: Some fabricated RF structures using ESL41110 materials

In this section, we first describe the fabricated LTCC circuits that include transmission lines and microstrip resonators discussed in the previous section. Measurement results as well as the dielectric parameters extraction of ESL41110 is then presented.

3.3.1 Fabrication

Figure 3.22 shows the fabricated circuits that contain microstrip line and resonators. Each circuit is composed of six ESL41110 layers. The first two circuits ((a) and (b)) represent the simulated resonators "Ring 1" and "T1" while the third contain the microstrip line "Line 1" and resonators "Ring 2" and "T2". A TRL kit is added to the circuits for measurement calibration.

For the manufacturing, the LTCC layers are cut with dimension of $50.8 \times 50.8\ mm$ and stabilized at $80°C$ during 30 minutes. Ground vias (for interconnecting connectors to ground plane) are created using the laser system ASTREE 250 and then filled by the ESL802 gold conductor. Next, the different patterns as well as the ground plane are screen printed using the ESL803 paste conductor. The gold-platinum 5873-G paste is also deposited on the top layer for SMP connector footprints. The LTCC layers are manually stacked and then pressed at $70°C$ and 200 $bars$ for 10 minutes cutting halfway through before firing. Finally, the circuits are fired in the box furnace using ESL41110 firing profile.

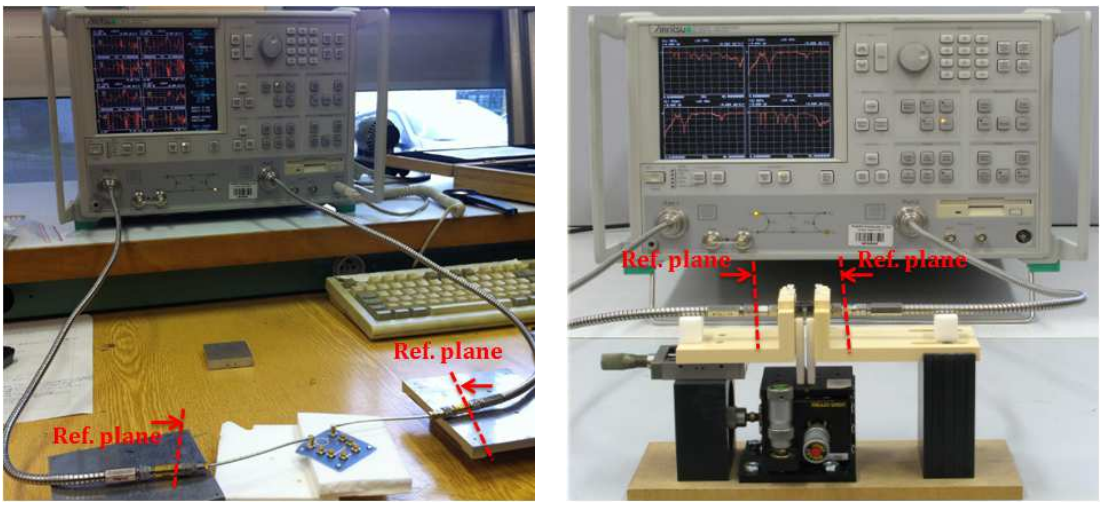


(a) (b) (c)

Figure 3.22: Fabricated circuits on six ESL41110 layers: (a) Ring resonator "Ring 1". (b) T-junction resonator "T1". (c) Microstrip line "Line 1" and resonators "Ring 2" and "T2"

3.3.2 Measurement

After firing, the different parts of LTCC circuit shown in Figure 3.22-(c) are broken by manual operation. Then, the different structures are dimensionally measured with the 3D optical microscope shown in Figure 2.25. Finally, the RF characterization in terms of S-parameters of different elements is carried out using the Vector Network Analyzer (VNA) 37397C (40 MHz-65 GHz) from ANRITSU. For circuits with SMP connectors, a transition from V to SMP connector (Figure 3.23-(a)) is used while for the others, the measurement is achieved using the test fixture shown in the Figure 3.23-(b). We note that this fixture, that use coaxial connectors up to 40 GHz from SOUTHWEST MICROWAVE, is developed in the laboratory in order to avoid braking the LTCC circuit during measurement (see section 2.4.8). Finally, the SOLT calibration is made at the reference planes represented on Figure 3.23 because the TRL calibration is not perfect due to the difficulty to ensure repeatable contacts in the test fixture for all the LTCC calibration standards.



(a) (b)

Figure 3.23: RF measurement of LTCC circuits: (a) Using the SMP connectors. (b) Using the test fixture

3.3.2.1 Microstrip line

Table 3.5 shows the measured dimensions of microstrip line "Line 1" (section 3.2.2.1) after fabrication. The line geometry is slightly affected by the shrinkage occurred during the LTCC circuit processing. These new values are taken into account during the retro-simulation of the structure.

Table 3.5: 50 Ω microstrip lines geometry

Parameter	Designed	Fabricated
h_{ms}	450 μm	450 $\pm$ 10 μm
w_{ms}	880 μm	900 $\pm$ 10 μm
L_{ms}	12.5 mm	12.47 mm

The RF measurement is made using the microstrip test fixture up to 40 GHz. Figure 3.24 compares the measurement results (black) to the simulation results (red), while the green curve shows the retro-simulation results where the fabrication tolerances and the coaxial to microstrip transitions of SOUTHWEST connectors are taken into account.

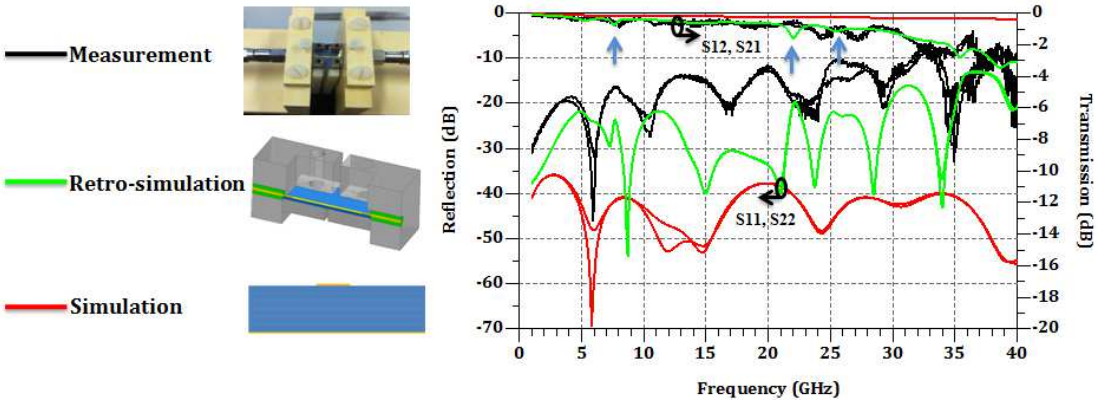


Figure 3.24: Measurement, simulation and retro-simulation results of microstrip line up to 40 GHz

The measurement results fit to retro-simulation results (with connectors effect) in term of transmission and the return losses. The return loss is better than 10 dB and the transmission loss is in the order of 1.5 dB up to 30 GHz.

The resonances in the transmission loss curve (blue arrows) are due to the cavity created by the test fixture with its coaxial connectors as shown by measurement and retro-simulation. To validate this statement, an EIGENMODE solution for cavity resonance identification is made with HFSS®. Figure 3.25 shows the resonance modes in the cavity created by the test fixture.

The measurement of the fabricated microstrip line "Line 2" (Figure 3.21 - A) is not completed due to a parallel plate mode (at about 25 GHz) created between the bottom and the intermediate ground planes. To suppress this mode, the distance between the ground vias and the ground plane edge must be reduced.

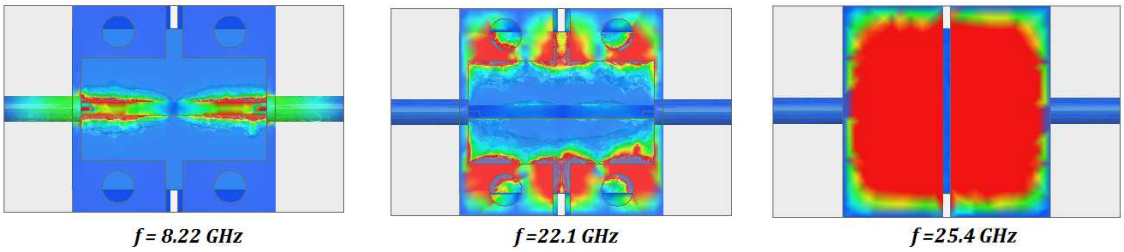


Figure 3.25: Resonance frequencies in the cavity created by the coaxial connectors of test fixture

3.3.2.2 Conductor Backed Coplanar Waveguide

Figure 3.26 shows the measurement results of the CBCPW line simulated in section 3.2.2.2 from 1 to 20 GHz. A comparison between simulation and retro-simulation results is also illustrated. The spacing between the center conductor and lateral ground planes (S_{cpw}) are affected by the fabrication tolerances of 10 μm (110 μm relative to 120 μm designed). The return and transmission losses are better than 18 dB and 1 dB up to 20 GHz respectively.

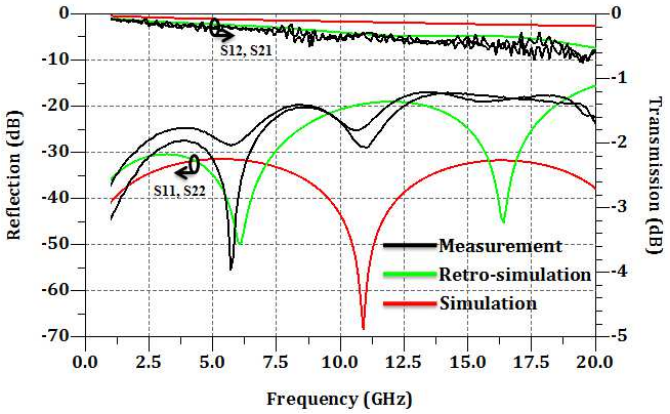
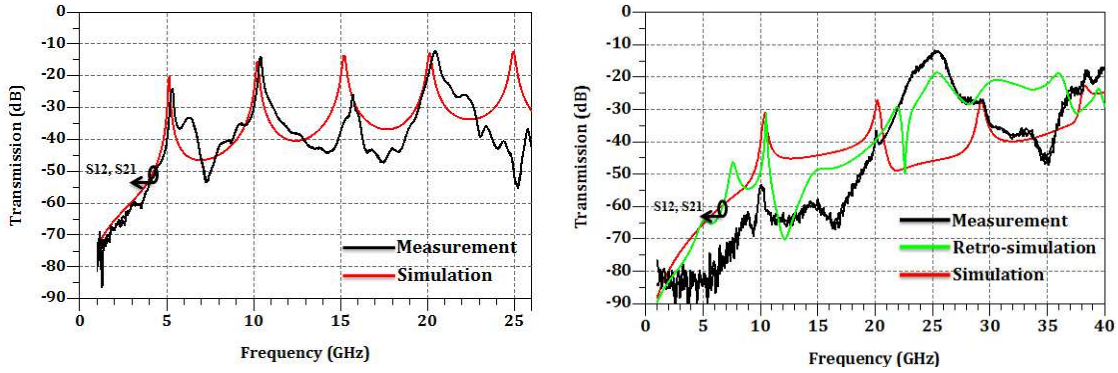


Figure 3.26: Measurement, simulation and retro-simulation results of the CBCPW line up to 20 GHz

3.3.2.3 Ring resonator

The ring resonators "Ring 1" and "Ring 2" simulated in section 3.2.3 are characterized in term of transmission factor using the two measurement techniques presented previously. The first is measured using the SMP to V transition (Figure 3.23-(a)) up to 26 GHz, while the second is characterized in the microstrip test fixture (Figure 3.23-(b)) up to 40 GHz. We also note that after circuits fabrication, the measured mean radius of "ring 1" is 4.99 mm (designed to be 5 mm) and the gap width is 125 μm (designed to be 120 μm). For the "Ring 2", the mean radius is 2.61 mm (designed to be 2.6 mm) and the gap width is 450 μm (designed to be 450 μm). These tolerances and the connectors effect on the "Ring 2" are taken into account in the retro-simulations.

The measurement, simulation and retro-simulation (for "Ring 2") results of the transmission factor are shown in the Figure 3.27.



(a) Ring 1 (b) Ring 2

Figure 3.27: Transmission factor measurement of microstrip ring resonators

Analyzing these results, the measured resonant frequencies are relatively close to those obtained in simulation. We can see fluctuations on the measured results of "Ring 1" (left). This is due to the effect of the two coaxial cables presented in the SMP to V transition (SOLT calibration made at the transition entry). In the second ring (right), the cavity mode generated by the connectors in the test fixture appears at several frequency and is clear at 25.3 GHz (at the peak of the transmission factor). Figure 3.28 shows this resonance identified by EIGENMODE solution in HFSS®.

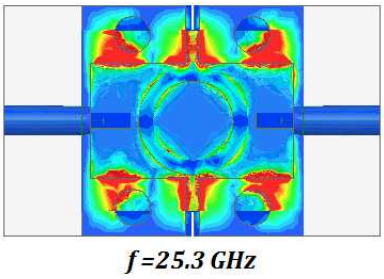


Figure 3.28: Resonance mode in cavity created by coaxial connectors at 25.3 GHz

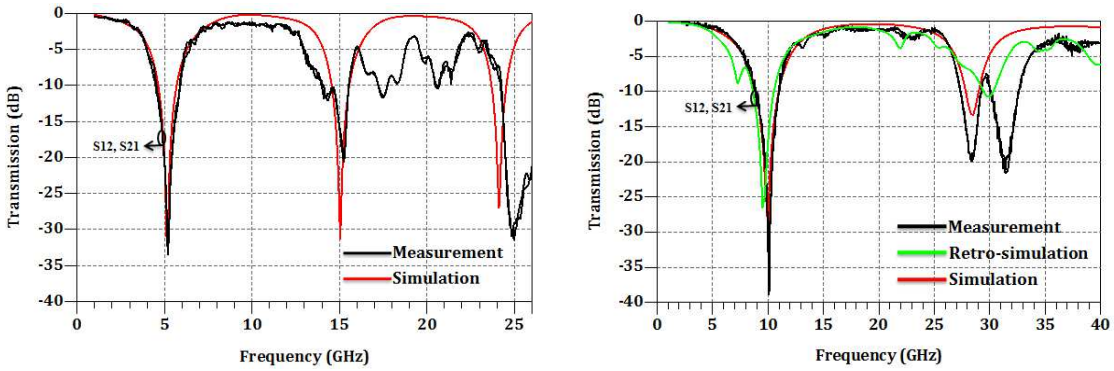
Table 3.6 shows the extracted ESL41110 material parameters at the resonant frequencies of the both "Ring 1" and "Ring 2". The effective permittivity is calculated from Equation 3.24 while the dielectric constant is deduced from Equation 3.1. The others parameters are calculated by equations discussed in section 3.1.2. The dielectric constant varies from 4.2 to 4.7 between 5 and 29 GHz which is close to that value from ESL (see Appendix B ESL41110 data sheet). For the total attenuation, the values are different for both resonators because of the difficulty to obtain an accurate value of 3 dB bandwidth. This is due to the lack of a TRL calibration and the loss in the coaxial cables and connectors where it is impossible to estimate a precise value of the attenuation in the resonators.

Table 3.6: Microstrip ring resonator parameters extraction

Parameter	Ring 1				Ring 2		
	$n=1$	$n=2$	$n=3$	$n=4$	$n=1$	$n=2$	$n=3$
Frequency(GHz)	5.35	10.42	15.7	20.25	10.2	20.1	29.3
Transmission factor (dB)	−24.14	−14.15	−25.85	−12.42	−54.35	−36.4	−27.5
3dB bandwidth (GHz)	0.18	0.2	0.17	0.41	0.5	0.27	0.75
Effective permittivity	3.19	3.37	3.33	3.57	3.21	3.32	3.5
Deduced dielectric constant	4.2	4.4	4.36	4.7	4.21	4.4	4.65
Loaded quality factor	29.7	52.1	92.4	49.3	20.4	19.83	39.06
Unloaded quality factor	31.66	64.8	97.2	64.4	20.43	20.13	40.77
Attenuation factor (dB/m)	3.16	3.09	3.1	6.22	11.6	23.6	17.5

3.3.2.4 Microstrip T-junction

Similarly, the two microstrip T-junctions "T1" and "T2" are measured in terms of transmission factor up to 26 GHz and 40 GHz respectively. The same measurement techniques used in the ring resonators are used to characterize the T-junctions resonators. The measurement, simulation and retro-simulation (for "T2") results are shown in the Figure 3.29. We note that after fabrication the stub length L_{stub} of "T1" and "T2" are 7.9 mm (8 mm designed) and 4.06 mm (4 mm designed) respectively.



(a) T1 (b) T2

Figure 3.29: Transmission factor measurement of microstrip T-junction resonators

The measured resonant frequencies shown in the previous figure are close to the simulation and retro-simulation of T-junction resonators. As explained in the measurement of ring resonators, the fluctuations and the cavity resonance modes are caused by the coaxial cables and test fixture respectively.

Table 3.7 shows the frequency values and the extracted relative permittivity calculated from Equation 3.29. The deduced dielectric constant at 28 GHz exceed 5 and is different to that obtained previously in the measurement by the ring resonator (4.65 at 29.3 GHz). The problem

can be related to the measurement (cavity created by the test fixture) that affect the resonance frequency or to the fabrication tolerances (the stub length is different to 4.06 mm).

Table 3.7: Microstrip T-junction resonator parameters extraction

Parameter	**T1**			**T2**	
	$n=1$	$n=3$	$n=5$	$n=1$	$n=3$
Frequency(GHz)	5.17	15.28	24.9	10.1	28.3
Transmission factor (dB)	−33.19	−20.71	−30.7	−38.9	−19.92
3dB bandwidth (GHz)	0.11	0.24	0.49	0.08	0.68
Effective permittivity	3.37	3.48	3.63	3.34	3.8
Deduced dielectric constant	4.47	4.65	4.83	4.44	5.07
Loaded quality factor	46.4	63.6	50.8	126.3	41.6
Unloaded quality factor	47.4	70.9	52.3	127.7	22.36
Attenuation factor (dB/m)	8.3	16.8	38	6.05	103.8

Finally, we plot on Figure 3.30 the deduced dielectric constant from various measurement techniques. As this figure implies, the dielectric constant falls between 4 and 5 up to 30 GHz. Measurement results of "Ring 1" (blue curve) is the closest to that measured by ESL (dashed line) below 20 GHz. The permittivity extracted at frequencies over 20 GHz might not be correct due to the poor measurement quality. The dissipation factor of the ESL41110 LTCC material is not extracted due to the coaxial cable and connector losses.

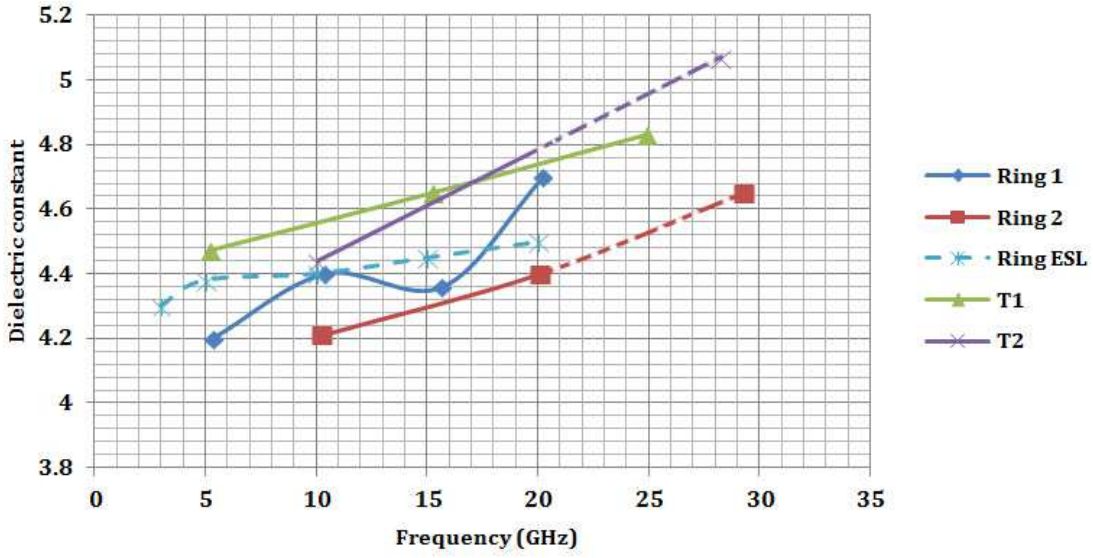


Figure 3.30: Deduced dielectric constant from various measurement methods

3.4 LTCC characterization in the W band

As shown in the previous section, the material characterization using resonant methods is limited to a specific discrete frequency. In addition, the characterization by waveguide or cavity methods becomes complex at millimeter wave frequencies due to the circuit dimensions and manufacturing limitations. To address these limitations, a solution based on a free-space (or quasi-optical) method to extract the ESL41110 material parameters up to the W band can be used. The main advantage of this method is that it does not require complex circuit fabrication (*e.g.* microstrip resonators) or specific machining of slab samples. Furthermore, broadband measurements can be achieved. The principle consists of inserting the dielectric substrate into a free space transmission path between two focusing lens antennas and then measuring the material scattering parameters to extract the complex permittivity from the four S-parameters.

Figure 3.31 shows the measurement setup of the quasi-optical bench developed in our laboratory [20]. This bench contains two Gaussian Optics Lens Antennas (GOLA) that are designed to radiate a paraxial beam to ensure plane wave along the propagation axis. It is also composed of a sample holder used to maintain the substrate material, X, Y and Z positioners with 10 μm precision, an ABMM VNA and a computer for permittivity calculations.

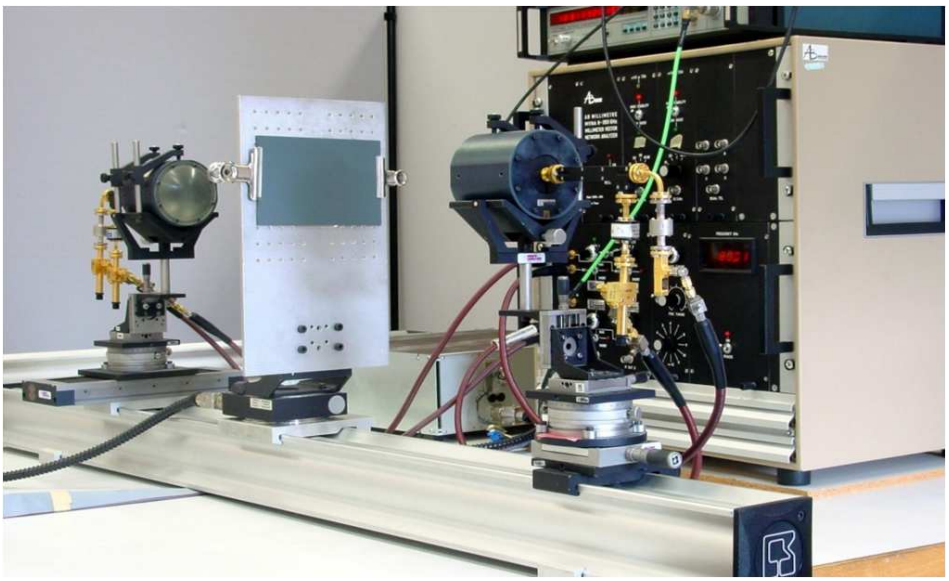


Figure 3.31: Quasi-optical test bench for dielectric material extraction in the W frequency band

A TRL calibration technique is used to move the reference planes to the material interfaces. An explanation of the calibration technique as well as the extraction parameter calculations are detailed in [20]. The extraction of complex dielectric permittivity is based on the S_{21} parameter and S_{11} is used for verification. The analytical S_{21} and S_{11} of infinite material under plane

wave assumption are:

$$S_{21} = S_{12} = \frac{(1-\rho^2)e^{-j\Gamma h}}{1-\rho^2 e^{-2j\Gamma h}} \tag{3.30}$$

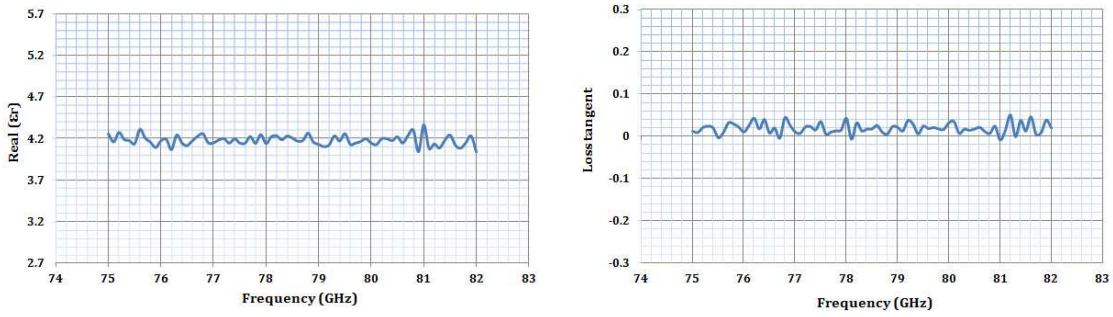
$$S_{11} = S_{22} = \frac{\rho(1-e^{-j\Gamma h})}{1-\rho^2 e^{-2j\Gamma h}} \tag{3.31}$$

with:

$$\begin{cases} \rho = \frac{1-\sqrt{\varepsilon_r}}{1+\sqrt{\varepsilon_r}} & \Gamma = \frac{2\pi}{\lambda_0} \\ \varepsilon_r = \varepsilon_r' + j\varepsilon_r'' = \varepsilon_r'(1-tan\,\delta) \end{cases} \tag{3.32}$$

where λ_0 is the free-space wavelength, h is the substrate thickness, and the loss tangent is calculated by $tan\,\delta = -\frac{\varepsilon_r''}{\varepsilon_r'}$ with $\varepsilon_r' < 0$. The ε_r is determined from the complex S_{21} parameter using an optimization procedure.

The test sample used for characterization is composed of three layers ($h = 245\ \mu m$) of ESL41110 LTCC material. The substrate dimension is about $11\ cm \times 11\ cm$. The LTCC material is placed between the two lens antennas and the measurement is achieved between 75 and 82 GHz. Figure 3.32 shows the measured relative permittivity (ε_r') and loss tangent ($tan\,\delta$).



(a) (b)

Figure 3.32: Permittivity extraction of the ESL41110 substrate material: (a) Relative permittivity (ε_r'). (b) Loss tangent ($tan\,\delta$)

Finally, the average values of dielectric constant and loss tangent are calculated according to the extracted real and imaginary parts of the relative permittivity. The average dielectric constant of the ESL41110 material is 4.18, which is close to the ESL value and the dissipation factor is about 0.018 (0.004 at 1 MHz from ESL).

3.5 "mm-packaging" project

The project MM-PACKAGING, which aims at the integration of GaAs MMICs in an LTCC package intended for millimeter wave applications was performed in collaboration with the Microwave Electronics Laboratory of CHALMERS UNIVERSITY OF TECHNOLOGY - (GÖTEBORG, SWEDEN).

The main objectives of this project are:

- The conservation of the desirable RF properties of the MMIC
- The miniaturization of LTCC package
- The validation of LTCC technology for fabrication of multilayer RF structures

In this section, we describe the design, implementation and validation of a multilayer LTCC package that integrates a Voltage Controlled Oscillator (VCO) fabricated in MMIC technology. The frequency operating bandwidth of the VCO (Figure 3.33) is 2 GHz (10.6 – 12.6 GHz) with a phase noise of about −105 dBc/Hz at 100 kHz. The chip presents a single RF output and three DC bias inputs for varactor, collector and base. The chip dimensions are 1872 × 1972 × 75 μm.

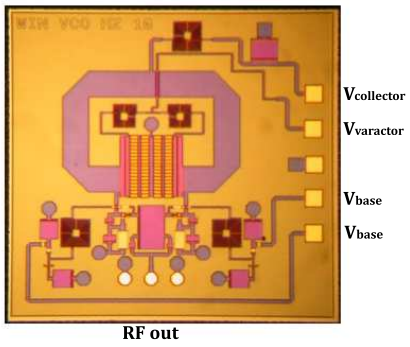


Figure 3.33: The VCO chip fabricated in MMIC technology

3.5.1 Package design

Figure 3.34 gives a 3D view of the LTCC package of the MMIC VCO presented above. In this section, present the design of the different package elements which includes the RF, DC and cavity parts. The first point is devoted to the design and optimization of generic transition from CBCPW line to stripline. Then, we analyze the wire bonds and matching network necessary for impedance compensation. Cavities and resonance identification is also presented and next, the RF performance of the complete RF transition in terms of S-parameters is presented. Finally the DC part of the package is discussed. The ESL41110 LTCC material is used as substrate and ESL802 and ESL803 gold are used as conductors. The metalization thickness is 6 μm and the package design is based on the DESIGN RULES discussed in section 2.5.

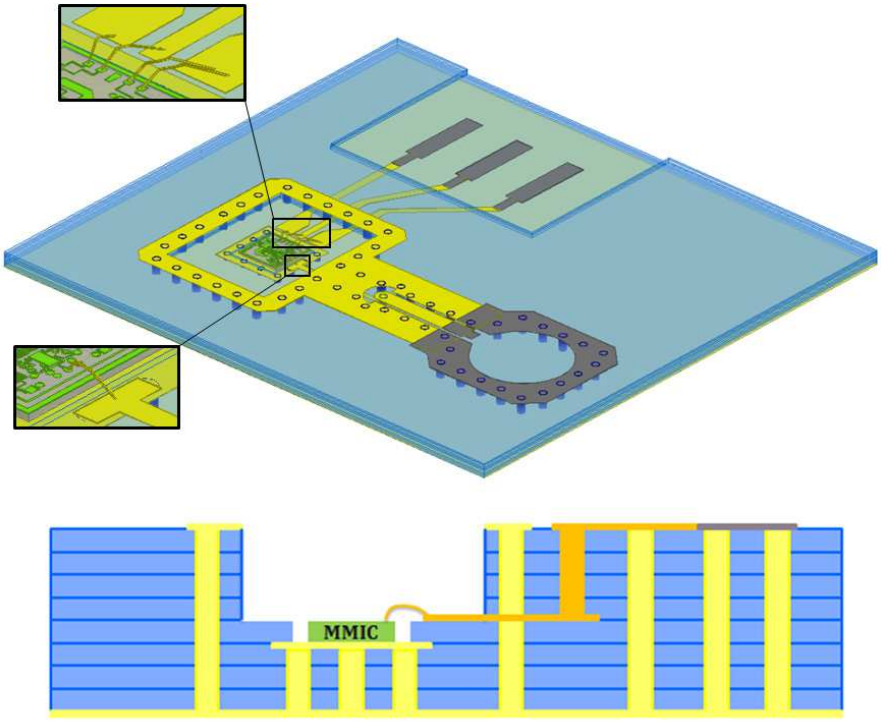


Figure 3.34: 3D view and cross section of LTCC package for MMIC VCO in eight ESL41110 LTCC layers

3.5.1.1 CBCPW to stripline transition

In this section, we will describe the design of LTCC CBCPW to stripline transition in detail, and then present the results of the electromagnetic analysis using HFSS®.

Figure 3.35 shows the cross section of the transition named CBCPW-SL between a CBCPW line placed on the surface of the package, and a stripline embedded inside the substrate. The study is conducted in a back-to-back configuration that means the transition is composed of two CBCPW lines through a stripline line (CBCPW-SL-CBCPW). A back-to-back configuration allows us to test the transition's S-parameters. We also note that only one half of the structure is calculated in EM simulation in order to reduce the computation time by taking into account the magnetic plane of symmetry.

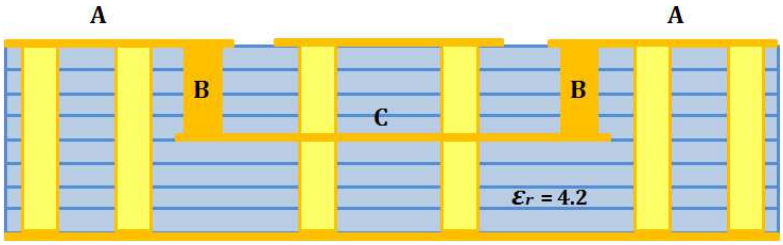


Figure 3.35: Cross section of back to back CBCPW-SL-CBCPW transition

For the design, the transition is implemented on eight ESL41110 layers with a permittivity of 4.2 and a loss tangent of 0.004 (at 1 MHz). As shown in the Figure 3.35, the transition is composed of three elements, the CBCPW line (A), the stripline (C) and the vertical interconnection between the two lines (B). To predict the performance of the complete transition, we first analyze these elements separately. Then, we optimize these structures to obtain a return loss better than 20 dB between 10.6 and 12.6 GHz. The two transmission lines (CBCPW and stripline) as well as the vertical transition are designed to get a 50 Ω characteristic impedance. Ground vias with 220 μm of diameter and 750 μm of space are used to interconnect the two ground planes in order to suppress the higher-order modes excited at higher frequencies. The transition between the CBCPW and the stripline is achieved through a via which is present on four LTCC layers. The diameter of the signal via is optimized according to space of ground vias placed around the signal via to obtain optimum coaxial effect. The characteristic impedance of a coaxial line, in the case of low loss and high frequency, is given by Equation 3.33.

$$Z_c = \frac{138}{\sqrt{\varepsilon_r}} log \frac{d_2}{d_1} \tag{3.33}$$

where d_1 is the diameter of the signal via and d_2 is the diameter of the opening created by ground vias.

A one half circular opening is also created in the top ground plane. The size of this opening (R_{hole}), the via signal catch pad and the ground via location are optimized using parametric analysis to obtain better performance in terms of S-parameters. Figure 3.36 shows the geometry and dimensions of the CBCPW-SL transition.

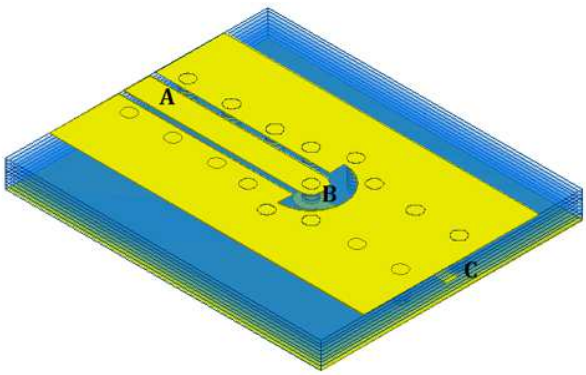
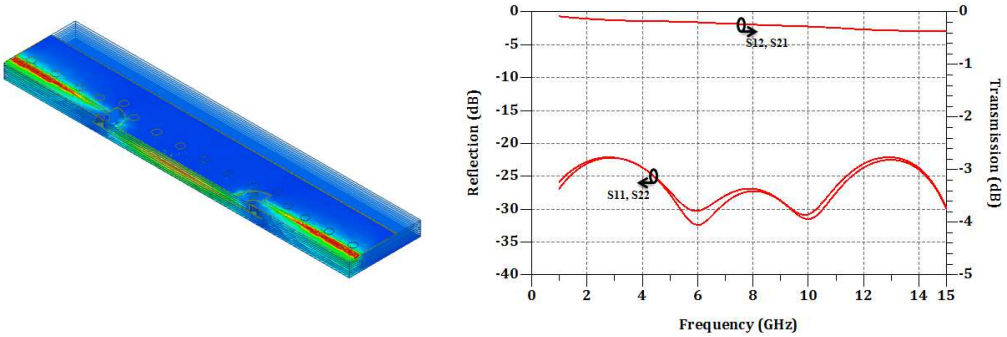


Figure 3.36: CBCPW-SL geometry: (a) CBCPW line: $w_{cpw} = 590\ \mu m$, $s_{cpw} = 120\ \mu m$, $w_{gcpw} = 2\ mm$, $h_{cpw} = 600\ \mu m$ and $L_{cpw} = 4\ mm$. (B) Coaxial line: $d_1 = 0.3\ mm$, $d_2 = 1.75\ mm$ and $R_{hole} = 0.6\ mm$.(C) Stripline: $w_{sl} = 280\ \mu m$, $w_{sl} = 280\ \mu m$, $h_{sl} = 220\ \mu m$ and $L_{sl} = 3.44\ mm$

The transition's S-parameters are simulated between 1 and 15 GHz in a back-to-back configuration. The E-field at 11 GHz and the RF performance in return and transmission losses are presented in Figure 3.37. The performance is better than 20 dB and 0.3 dB in return and transmission losses respectively.



(a) (b)

Figure 3.37: EM simulation of back to back CBCPW-SL transition: (a) E-field at 11 GHz. (b) S-parameters results

3.5.1.2 Bond wire and matching network design

The wire bond interconnect is used to transfer the RF signal from the MMIC to the package. A bond wire behaves as an inductor at higher frequencies and the characteristic impedance increases and requires matching to deliver maximum power from the source to the load and to eliminate undesired reflections. Several matching techniques including lumped elements and stub tuners are used and discussed in [1]. In this section, we present the design and simulation of round and ribbon bonds and their matching networks.

The simulated bond wire geometry is shown in Figure 3.38. The chip is placed in a cavity in order to minimize the bond wire length. The parameters that affect the RF performance are the wire diameter (ϕ_b) for round wire or the cross section width for ribbon ($w_b \times t_b$), wire length (L_b), height (h_b) and start (α) and end (β) angles. EM simulation of these structures is performed with HFSS between 1 and 20 GHz. The round wire diameter is 25.4 μm while the ribbon width and thickness are 50 μm and 12 μm respectively. The bond length is 730 μm that includes the distance from chip pad to chip edge, the gap between the chip and the cavity edge, and the distance between the cavity edge and bond pad on the package. The height is about 120 μm and the angles (α and β) are about 20°.

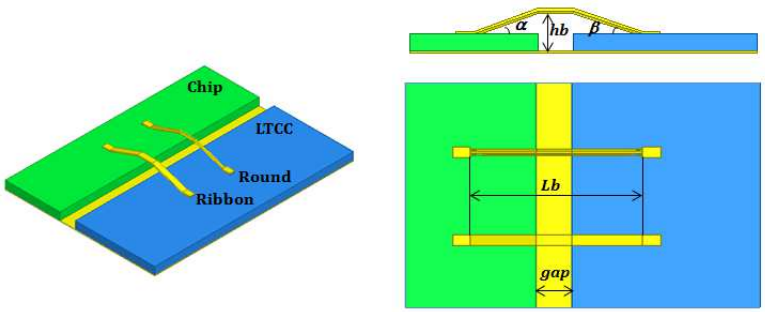
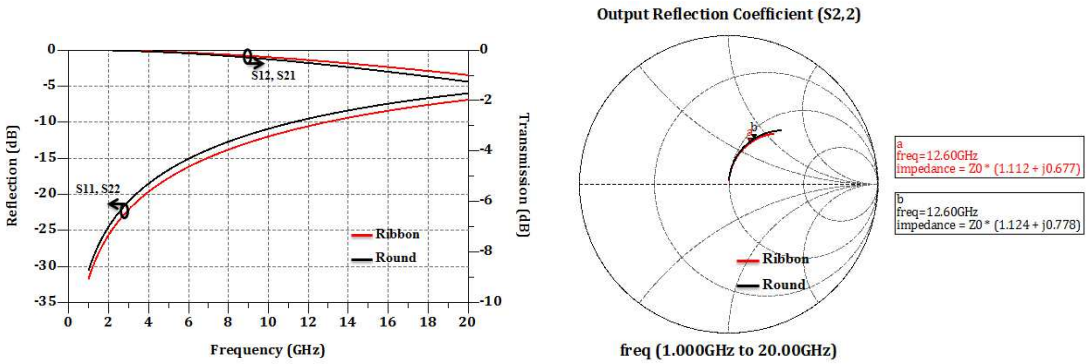


Figure 3.38: Simulated round and ribbon bond wires for interconnect chip to package: $L_b = 730\ \mu m$, $h_b = 120\ \mu m$, $\alpha = 20°$ and $\beta = 20°$, $\phi_b = 25.4\ \mu m$, $w_b = 50\ \mu m$, $t_b = 12\ \mu m$ and $gap = 150\ \mu m$

Simulation results illustrated in Figure 3.39 show that the ribbon bond is slightly better than round bond wire, but beyond 10 GHz the two bond wires present a return loss less than 10 dB. Since the operating frequencies of our VCO is above 10 GHz, a matching network is required in order to improve the performance. The SMITH chart shows the impedance at the end of wire bonds (package side) at 12.6 GHz.

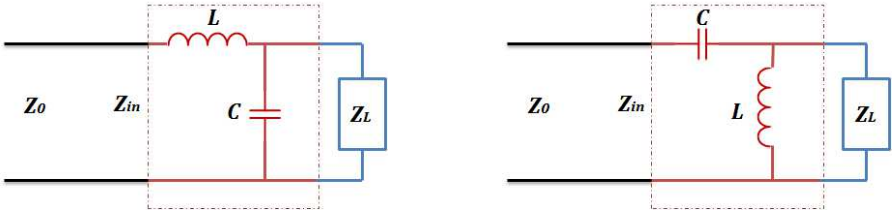


(a) (b)

Figure 3.39: Round vs ribbon bond wires simulation results: (a) S-parameters. (b) Smith chart

The bond wires presented above are matched with lumped elements (LC network) method. This method is the simplest type of matching network which uses two reactive elements to match load impedance to a transmission line [1]. Two configurations are used (see Appendix C), which depend on the load impedance location relatively to the $1+jx$ circle on the SMITH chart. If the normalized load impedance $z_L = Z_L/Z_0$ is inside $1+jx$ circle the circuit of Figure C.1-(a) is used. If the normalized load impedance is outside $1+jx$ circle the circuit of Figure C.1-(b) is used.

The load impedance at 12.6 GHz of round ($Z_{round} = 50(1.124+j0.778)\ \Omega$) and ribbon ($Z_{ribbon} = 50(1.112+j0.677)\ \Omega$) bonds are inside the $1+jx$ circle (Figure 3.39-(b)). The matching network of Figure C.1 is applied. The calculation of the reactive elements (X and B) is achieved using MATLAB®. As shown in Figure 3.40, two matching networks with L and C elements are obtained.



(a) Network 1 (b) Network 2

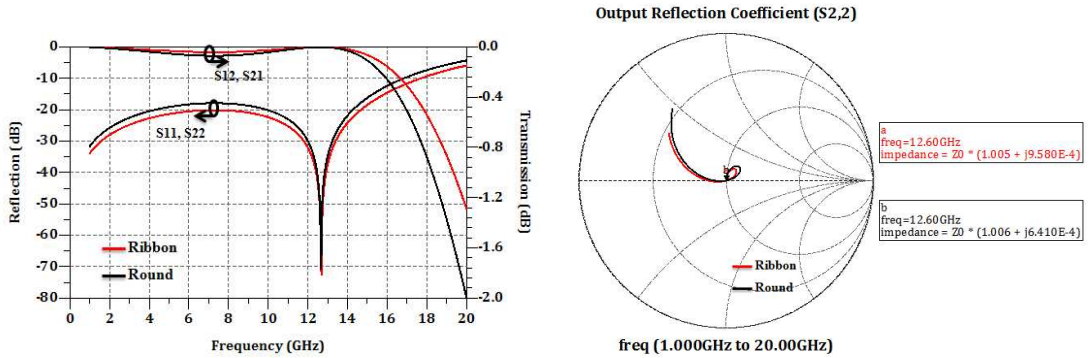
Figure 3.40: Two LC matching networks for z_L inside the $1+jx$ circle

Table 3.8 shows the calculated values of L and C for round and ribbon bonding for "Network 1" and "Network 2" matching circuits.

Table 3.8: Calculated L and C values for round and ribbon wire bonds matching networks

	Parameter	Round	Ribbon
Network 1	$z_L(\Omega)$	$50(1.124+j0.778)$	$50(1.112+j0.677)$
	$L(nH)$	0.514	0.457
	$C(pF)$	0.228	0.22
Network 2	$z_L(\Omega)$	$50(1.124+j0.778)$	$50(1.112+j0.677)$
	$L(nH)$	8.62	8.35
	$C(pF)$	0.31	0.348

The L and C of "Network 1" shown in Table 3.8 are selected for wire bonds matching because of the low values relatively to "Network 2". These values can be easily achieved with distributed elements. Figure 3.41 illustrates the round and ribbon bonds after matching with lumped elements (L and C) at 12.6 GHz.



(a) (b)

Figure 3.41: Round vs ribbon bond wires after LC matching using "Network 1": (a) S-parameters. (b) Smith chart

Finally, the matching network is designed and simulated using HFSS®. The chip is placed in a cavity at the fourth layer. In order to increase the shunt capacitor value, one layer substrate thickness (75 μm) is used while the inductor is placed above four layers (300 μm). A taper is used to match the line discontinuity and to access to the stripline (for CBCPW-SL transition).

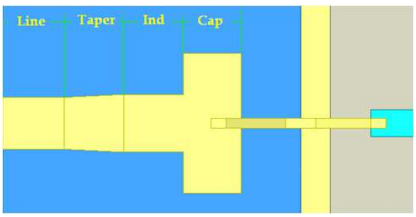


Figure 3.42: Distributed matching network design and dimensions for ribbon bond: Shunt capacitor $w_{cap} = 0.88\ mm$, $L_{cap} = 0.29\ mm$. Inductor $w_{ind} = 0.29\ mm$, $L_{ind} = 0.3\ mm$. Taper $L_{taper} = 0.31\ mm$. Line $w_{line} = 0.265mm$, $L_{line} = 0.31mm$

3.5.1.3 RF transition simulations

In this section, the RF signal of LTCC package is validated by EM simulation in back-to-back configuration. This signal combines the CBCPW to stripline transition and matching network described above. As shown in Figure 3.43, the transition is composed of eight ESL41110 layers. The MMIC chip which is represented here by a 50 Ω microstrip line is placed inside a cavity created at the fourth layer. The gap between the chip and cavity edge is 150 μm. An intermediate ground plane is deposited in the third layer for chip assembly. Ground vias are used to interconnect the both ground planes. A round wire bond with 25.4 μm diameter is used to interconnect the matching networks to 50 Ω microstrip line. Another cavity with 5.94 $mm \times 5.94$ mm is created at the top four layers.

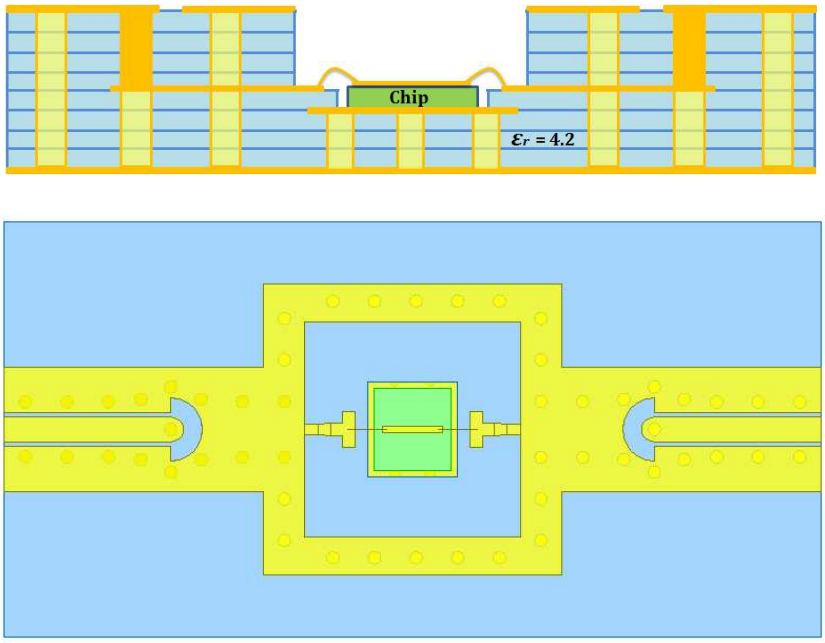
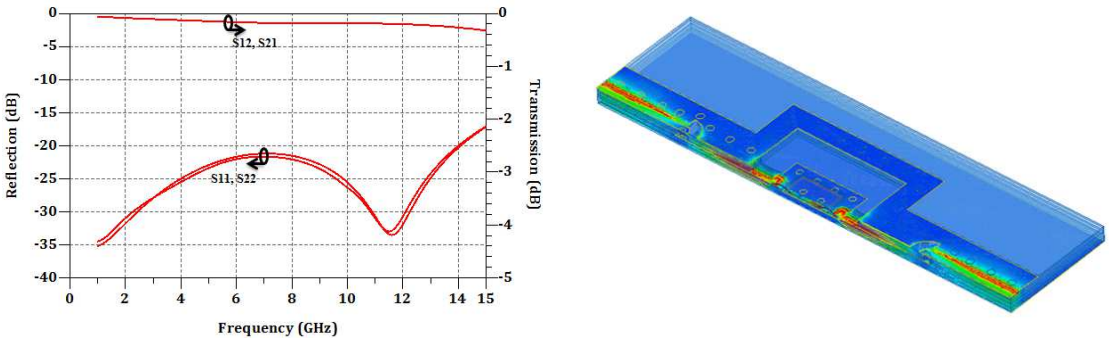


Figure 3.43: Cross section and top view of the LTCC package where the MMIC chip is replaced by a 50 Ω transmission line

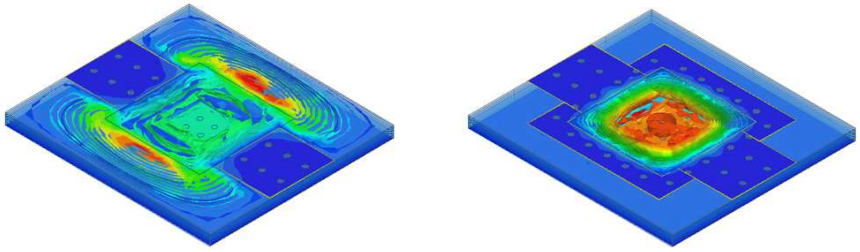
EM simulations of the RF transition are achieved between 1 and 15 GHz with HFSS® using wave port excitation. Simulation results as well as the E-field behavior of the transition at 11 GHz are shown in Figure 3.44. These results show a return loss (S_{11} and S_{22}) better than 20 dB between 10.6 and 12.6 GHz (MMIC oscillator frequency band). The transmission losses (S_{12} and S_{21}) are about 0.25 dB.

We note also that before the final design of the transition presented in Figure 3.43, cavity resonances are identified by EIGENMODE solution available in HFSS®. A ground plane section is added around the large cavity. The ground plane width and via positions are optimized to suppress parallel plate mode. As shown in Figure 3.45, the resonance frequency of the first mode is 19.6 and 25.4 GHz before and after adding ground vias respectively.



(a) (b)

Figure 3.44: RF transition simulation for VCO package: (a) S-parameters. (b) E-field at 11 GHz



(a): $f_{resonance} = 19.6\ GHz$ (b): $f_{resonance} = 25.4\ GHz$

Figure 3.45: E-field for the first mode resonance in RF transition cavities: (a) Before adding ground plane section and ground vias. (b) After adding ground plane and vias around the large cavity

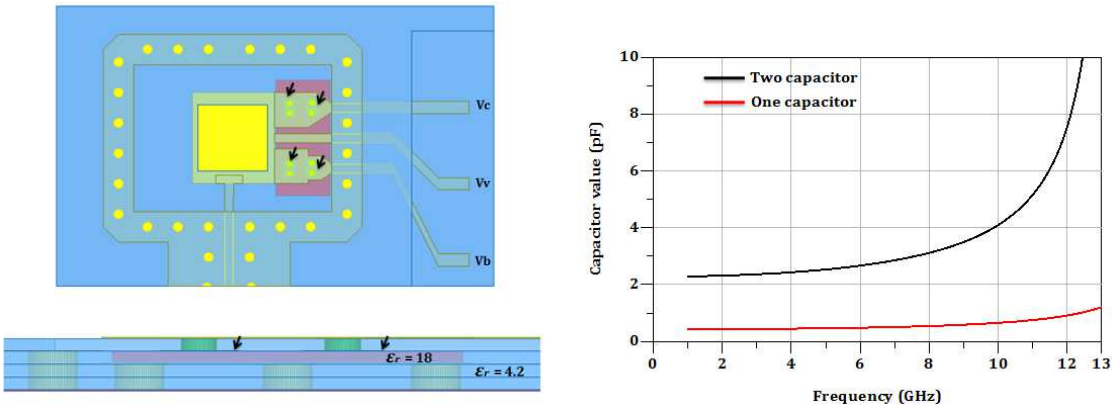
3.5.1.4 DC bias circuit simulations

Two DC voltages are used to bias the VCO, while a third DC voltage is used to variate the oscillating frequency. As shown in Figure 3.33, the VCO requires voltage for bipolar transistor bases, collectors and varactor diode. Three different prototypes were designed to include decoupling capacitor on the DC access (in addition to decoupling on the chip). The first prototype does not include any capacitors, the second allows SMD capacitors and for the last, MIM (Metal-Insulator-Metal) capacitors are integrated inside the ESL41110 substrate. The high permittivity dielectric material ESL41060 (ε_r of 18) is used for the insulation.

Figure 3.46-(a) shows the integrated capacitors connected to the collector and base lines. The second plate is represented by the ground plane. In order to increase the equivalent capacitance values, two capacitors that are in parallel, are connected on each line. The simulation is made in HFSS with one lumped port excitation. The equivalent capacitance values are optimized according to the plate size, vias diameter and spacing, and the DC pad size. Simulations of capacitors is made using HFSS® with one lumped port excitation. The equivalent capacitance value is calculated by Equation 3.34:

$$C_{eq} = \frac{-1}{imag(Z_{11})2\pi f} \tag{3.34}$$

Figure 3.46-(b) shows the calculated equivalent capacitance of simulated single and two parallel capacitors that are about 0.4 and 2.2 pF respectively.



(a) (b)

Figure 3.46: Integrated decoupling capacitor (black arrows) on DC lines: (a) Capacitor geometry. (b) Capacitor values

3.5.2 Package fabrication and measurement

Before the fabrication of the final LTCC package shown in Figure 3.34, the RF transitions presented previously are first fabricated in order to characterize their RF performances in terms of S-parameters. The tile layout shown in Figure 3.47 contains the CBCPW-SL and RF transitions in back-to-back configuration. A TRL (Thru-Reflect-Line) calibration kit is added to the layout and covers the frequency range between 1 and 30 GHz.

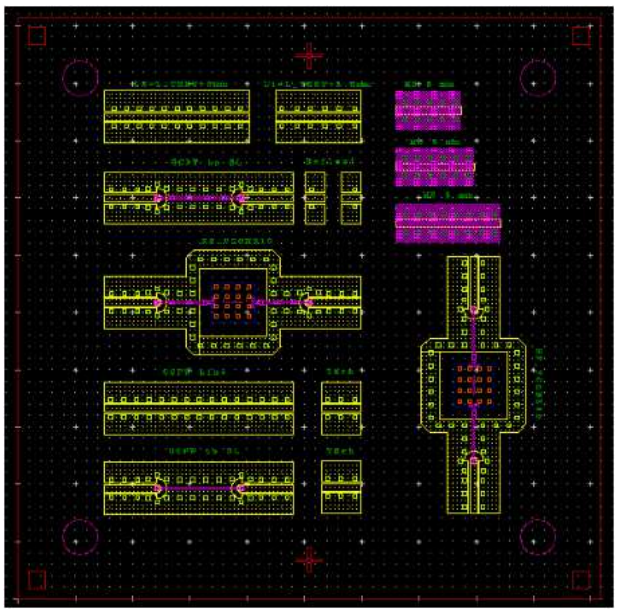


Figure 3.47: LTCC layout of multilayer RF transitions

The circuit processing is presented in Figure 3.48. The eight LTCC layers are first cut in $50.8 \times 50.8\ mm$ sheets and stabilized in oven. Then, the different vias and cavities are created using the ND-YAG laser system. The vias are filled and the patterns are deposited with ESL802 and ESL803 gold conductors using the standard thick film screen printer. During stacking, the fugitive ESL49000 material is inserted in the cavities to avoid the deformation during lamination. Selecting the recommended parameters, the circuit is uniaxially pressed and finally fired in the box furnace with the ESL41110 firing profile.

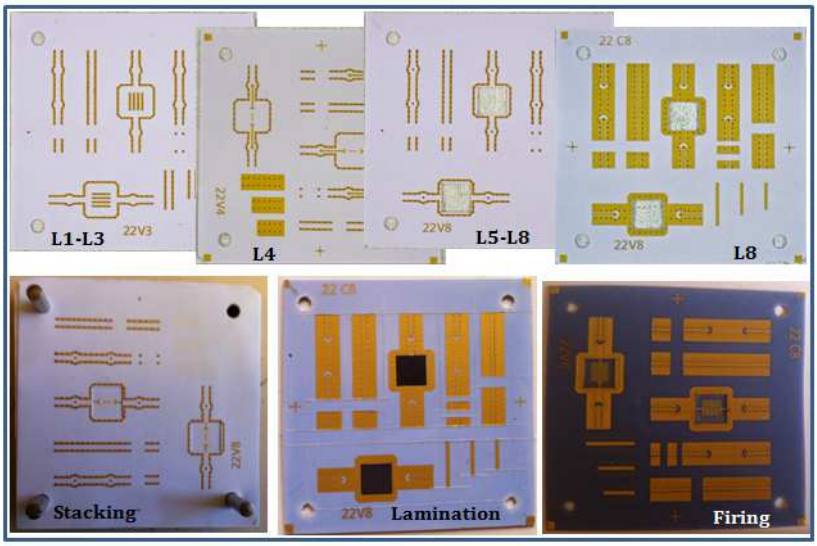


Figure 3.48: Fabrication process of RF transitions on 8 ESL41110 layers

After firing, the circuit is dimensionally measured using the 3D optical microscope. The shrinkage values are $13 \pm 1\%$ in x and y directions and $15 \pm 0.5\%$ in z direction. The fabrication tolerances of different patterns are about $\pm 10\ \mu m$. Finally, the circuit parts (Figure 3.49) are singulated at the precut edges and the round wire bonds with $25.4\ \mu m$ diameter are used to interconnect the $50\ \Omega$ microstrip line to the matching networks of the RF transition. The wire bond lenght is about $700\ \mu m$.

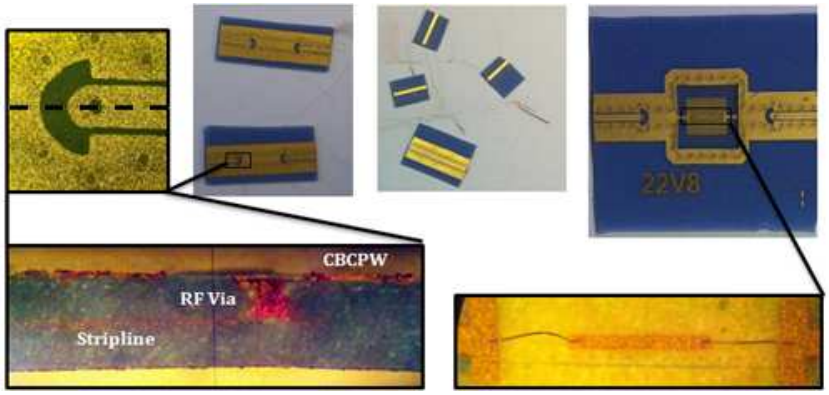


Figure 3.49: Singulated parts of fabricated LTCC circuits

The fabricated transitions simulated in section 3.5.1.1 and section 3.5.1.3 are measured in terms of S-parameters between 1 and 15 GHz using the VNA ANRITSU-37397C and the microstrip test fixture (Figure 3.23). Due to difficulties to ensure repeatable contacts during TRL standard measurements and LTCC circuit's fragility, the SOLT method for measurement calibration were used instead TRL method. The measurement, retro-simulation (with fixture connectors) and simulation results are shown in Figure 3.50. The measured return loss (S_{11} and S_{22}) for both transitions is better than 12 dB while the insertion loss (S_{12} and S_{21}) is about 1 dB (including the coaxial connector losses and in back-to-back configuration).

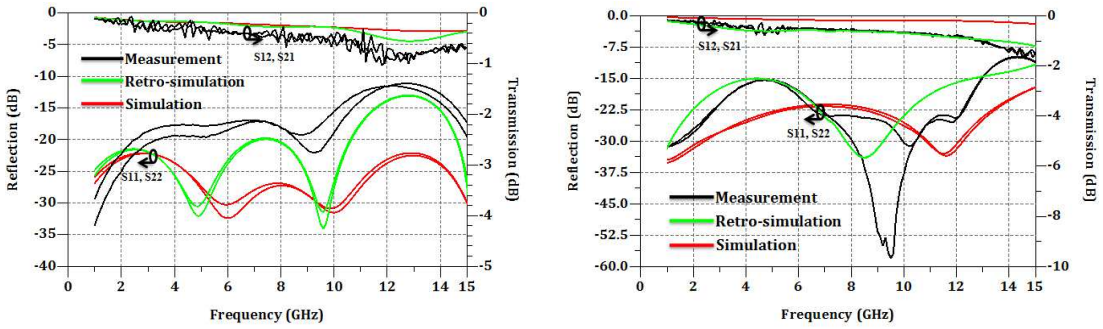


Figure 3.50: S-parameters measurement of multilayer RF transitions: (a) CBCPW-SL-CBCPW. (b) RF transition for VCO package

Once each of the transitions are validated, the LTCC package of the VCO is fabricated. The layout is shown in Figure 3.51 and it includes four LTCC packages with different DC parts as explained in section 3.5.1.4. The SMP footprint for connector assembly is added at the signal output of the three packages while the fourth package is designed to be measured in the test fixture.

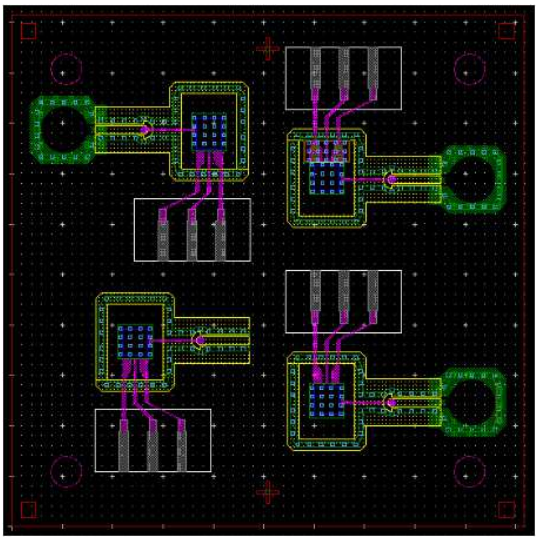
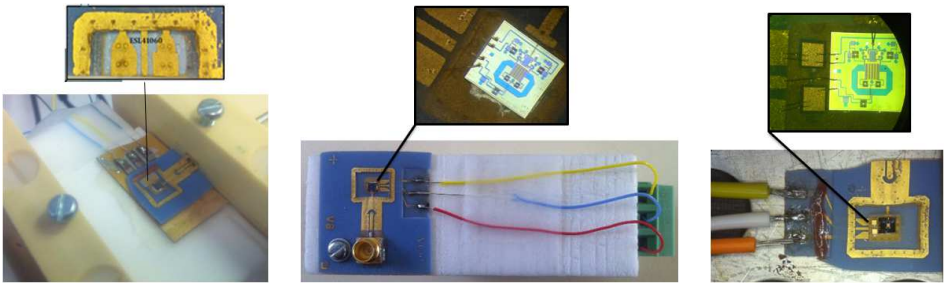


Figure 3.51: Layout of final LTCC packages

The circuit is processed in the same manner as the previous circuit. The high permittivity material ESL41060 is used as insert in the cavity. After firing, the circuit parts are cut and the MMIC chips as well as the SMD decoupling capacitors are mounted in the cavity using the conductive adhesive material H20E from EPOTEK. The connection between the chip and the package pads is made by gold wire bond with diameter of 25.4 μm and 700 μm in length (for RF signal). The surface mount SMP connectors [18] that operates up to 40 GHz are soldered on the top layer. Figure 3.52 shows the three packages after chip and wire bond assembly.



(a) (b) (c)

Figure 3.52: Final fabricated LTCC package: (a) With integrated MIM decoupling capacitors. (b) Without decoupling capacitors. (c) With SMD decoupling capacitors

The successful measurement in terms of the frequency band and output power of the packaged VCO is achieved with the two circuits without decoupling capacitors and with MIM integrated capacitors because the circuit with SMD capacitors broke when installing it in the measurement fixture. The measurement is carried out using the spectrum analyzer ROHDE & SCHWARZ FSQ (20 $Hz - 40$ GHz). A transition from V to SMP connector through a coaxial cable is used for RF signal output. The voltage on the base (V_b) and the collector must not exceed 3 and 7 V ($Ic = 35mA$) respectively. The varactor voltage (V_V) is variable between 0 and 14 V. The measurement setup is shown in the Figure 3.53.

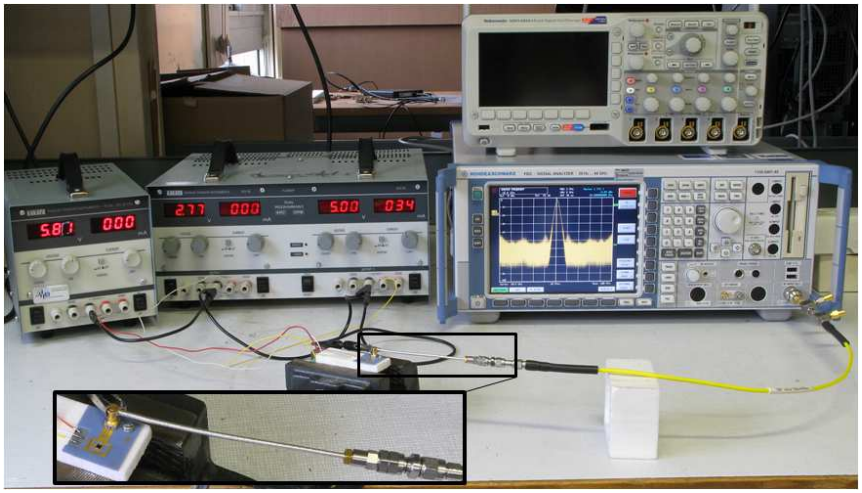


Figure 3.53: Measurement setup of frequency band of packaged MMIC VCO without capacitors

The measurement results of the two packaged MMICs illustrated in Figure 3.54 show variation of frequency band according to varactor voltage. As a comparison, on wafer MMIC measurement data is also presented. The DC bias on the base is the same but for the collector, the voltage is selected as a function of the current (Ic) in order to not exceed 35 mA. As this figure implies, the oscillation frequency varies between 10.1 and 12.4 GHz for a varactor voltage between 4 and 14 V. The measured output power is about $-2.4/-1.2$ dBm.

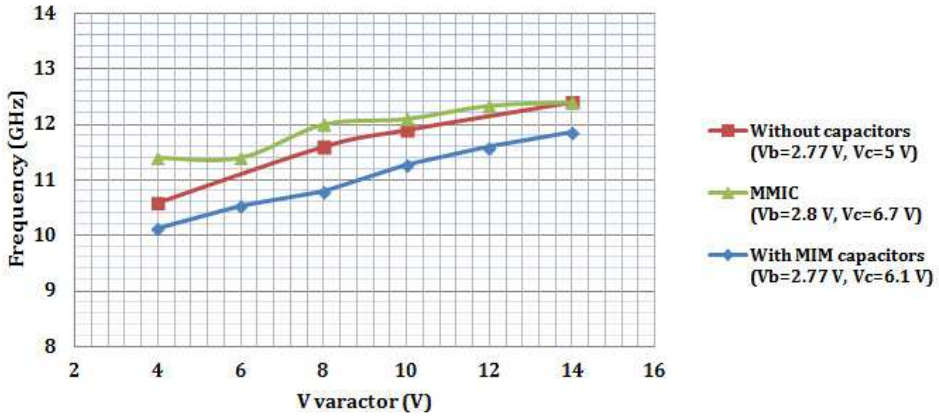


Figure 3.54: Frequency band measurement of packaged and unpackaged oscillators

When comparing the measurement data, the package without capacitors (red curve) shows similar results to the MMIC (green curve), while a frequency shift is observed for the package with MIM capacitors (blue curve). Indeed, it is possible to have differences from chip to chip where the chip (measured with probes) is not the same as the two packaged chips. We also note that the difference in the bias conditions, in terms of the collector voltage, down shifts the frequency by $1-2\%$. Finally, as the red and green curves are very close, we can presume that the MIM capacitors also influence the oscillating frequency.

Conclusion

In this chapter, we discussed the validation of LTCC technology in the RF domain up to 40 GHz. After a presentation of transmission line and planar microstrip resonator basic theory, we gave some results on RF structure simulations such as microstrip, CBCPW lines, ring and T-junction resonators using the ESL41110 LTCC material. The simulated structures were fabricated with the LTCC manufacturing process validated in chapter 2. After fabrication, we proposed a solution to measure the designed structures which were thereafter validated up to 40 GHz. Then, the MM-PACKAGING project regarding the integration of an MMIC oscillator in a multilayer LTCC package is presented. The design of the package parts such as a CBCPW-to-stripline transition, wire bonds and associated matching networks, DC bias circuits are presented. Finally, the multilayer transitions and the designed package VCO prototypes were fabricated and measured in terms of S-parameters and frequency bandwidth respectively.

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General conclusion

The development of new RF products is characterized today by a need of miniaturization, performance improvement and cost reduction. At the same time, the use of higher frequencies up to millimeter wave bands is always a development axis because it allows the use of larger frequency band and higher data rates. These constraints are strongly related to the packaging technology because it affects the electrical, thermal and mechanical performances of the microwave system. In order to meet these requirements, this thesis was conducted for introducing LTCC as a new packaging technology at LAB-STICC/TELECOM BRETAGNE up to millimeter wave frequency bands.

The research activities were concentrated in two directions: the technological direction that aims at the development and establishment of LTCC technology at TELECOM BRETAGNE for use in RF and microwave modules, and the RF direction which concerns the integration of an MMIC VCO in a multilayer LTCC package.

The bibliographic research achieved in chapter 1 presents the current packaging technologies used in the RF domain. This presentation concerns the study of the impact of the package on the MMIC performance, challenges and issues, and the evolution of RF packaging technology from SCP to SiP through MCM. The assembly methods of the MMIC chips are also illustrated. Secondly, a general owerview on LTCC technology was given. The evolution, material properties and the main features of LTCC are presented. Then, the LTCC is demonstrated as a good solution for RF packaging and microwave module applications. Finally, the recent state of the art of MMIC integration using LTCC was discussed.

In chapter 2, we presented the conducted activities to set up the LTCC technology in our laboratory. The chapter starts by the study of different LTCC materials on the market. The material from the American manufacturer ESL was selected to install this technology. This material is also selected taking into account the manufacturing process and maximum operating frequency limitations. Next, the LTCC manufacturing process validation using the available equipments in the laboratory has been presented. The work is based on more than fifty designed, fabricated and tested LTCC tiles. The process validation includes tape preparation, via and cavity formation, via filling, screen printing, stacking, lamination and firing. Then, the development of the technology has been evolved by resolving the different technological problems such as poor screen printed pattern, poorly via fill, uncontrolled shrinkage behavior,

circuit fragility and other difficulties encountered during the manufacturing process validation. At the end of this chapter, the elaboration of DESIGN RULES for future LTCC designers is presented.

In chapter 3, we first validated the LTCC technology in the RF bands up to 40 GHz. The work is based on the simulation and measurement results of some transmission lines and planar microstrip resonators. A theoretical study was given at the start of this chapter using the ESL41110 LTCC material. The simulation of different RF structures was made using ADS® and HFSS® software, while the measurement was achieved with a in-house developed test fixture and in some case using SMP connectors directly mounted on the top of the LTCC circuits. The measurement results was always close to that of the retro-simulation results and the extracted dielectric constant of ESL41110 varies from 4.2 to 4.8 between 1 and 30 GHz. Thanks to the MM-PACKAGING project, the design, simulation, fabrication and characterization of integrated MMIC VCO in a multilayer LTCC packages is then presented. This project was performed in collaboration with CHALMERS UNIVERSITY OF TECHNOLOGY, Göteborg, Sweden. The proposed package includes an RF and DC parts. The RF part that composed of a matched wire bond, a multilayer CBCPW-SL transition and SMP connector shows a performance better than 12 dB and 1 dB in return and transmission loss between 10.6 and 12.6 GHz respectively (including the connector loss and in back-to-back configuration). One of the packaged VCOs integrates decoupling capacitors using the ESL41060 LTCC material ($\varepsilon_r = 18$). Finally, the packaged VCO are measured. The oscillation frequency varies between 10.1 and 12.4 GHz for a varactor voltage between 4 and 14 V.

Perspectives

To pursue this work, many issues can be addressed, for instance the improvement of the LTCC manufacturing process, the measurement fixtures and increased complexity of the RF packages.

When it comes to the manufacturing process, dimensions have to be reduced in order to enable the use of higher operating frequency up to the millimeter wave range. The application of the photo-lithography process on LTCC minimizes the screen printing dimensions and tolerances (on the top layer) and allows us to have line widths and spaces down to 20 μm (relatively to $100-120$ μm in screen printing). Our fabrication process can be improved by the use of the isostatic pressing instead of the uniaxial pressing in order to better control the shrinkage after LTCC circuit firing. This would also diminish the cavity deformation during the lamination process. The low permittivity of the ESL41110 material allows the use of this tape up to millimeter wave bands without higher-order mode excitation, however its dissipation factor is rather high at 77 GHz (0.018). The use of other higher permittivity LTCC materials could also be explored.

To achieve the measurements, the test fixture developed in the laboratory for LTCC circuit measurements can be improved by using end launch connectors (from SOUTHWEST MICROWAVE) that operate up to 67 GHz. Furthermore, the development of photo-lithography process would enable the use of CPW structures on the ESL41110 substrate with fine line and space dimensions, which then would allow characterization of LTCC circuits in a probe station.

For RF packaging applications, the successful integration of an MMIC VCO in a multilayer LTCC package encourages us to go further up in frequency. Complex RF modules and SiP up to millimeter wave frequencies are to follow. For example, the project MM-PACKAGING can be extended to integrate both a VCO and a frequency multiplier by four to get an output frequency between 42 and 52 GHz. The MINI-SMP connectors that operate up to 65 GHz can be used to output the RF signal of such a module. Finally, a complete transceiver (amplifiers, mixer, antenna...) for 60 GHz band applications or a 77 GHz automotive radar system can be fabricated after these improvements.

Publications

Khodor Rida, Camilla Kärnfelt, Alain Peden, Guy Chuiton, Pascal Coant, Jean-Philippe Coupez, Herbert Zirath, Rumen Kozhuharov. Conception d'un boitier multicouche LTCC intégrant un Oscillateur MMIC. *Journnées Nationales Microondes 2013*, Paris, France, 14-17 Mai 2013.

Khodor Rida, Camilla Kärnfelt, Alain Peden, Jean-Philippe Coupez, Guy Chuiton, Pascal Coant. Radio Frequency Characterization of LTCC Materials in K and W Bands. *Giga-Hertz symposium 2012*, Stockholm, Sweden, 5-8 March 2012.

Appendix A

Appendix A: Substrate materials properties

A.1 Substrate materials properties

Table A.1: Electrical, thermal and mechanical properties of some substrate materials used in packaging technology

Material	Electrical				Thermal		Mechanical		
	DC[1]	LT[2]	ER[3]	BV[4]	TCE[5]	TC[6]	FS[7]	YM[8]	DN[9]
FR4	4.4	0.0200	–	50	15	0.3	–	370	–
Alumina (96%)	9.0	0.0002	$> 10^{14}$	8.3	6.5	24.7	352	370	3.98
Alumina (99%)	9.4	0.0001	$> 10^{14}$	8.7	6.8	28.1	331	344	3.92
Beryllia	6.4	0.0001	$> 10^{14}$	6.6	7.5	330	235	345	2.87
Aluminum nitride	8.9	0.0004	$> 10^{13}$	14	4.8	–	269	300	3.27
Dupont 951[10]	7.8	0.0015	$> 10^{14}$	> 1.1	5.8	3		152	3.1
Ferro A6M [10]	5.9	0.0020	$> 10^{12}$	> 5.0	4.5	2.5	> 170	92	2.45
ESL41110[10]	4.2	0.0040	$> 10^{12}$	> 1.2	6	2		–	–

[1] Dielectric Constant
[2] Loss Tangent
[3] Electrical Resistivity ($\Omega.cm$)
[4] Breakdown Voltage (kV/mm)
[5] Thermal Coefficient of Expansion ($ppm/^{\circ}C$)
[6] Thermal Conductivity ($W/m.^{\circ}K$)
[7] Flexural Strength (MPa)
[8] Young Modulus of elasticity (GPa)
[9] Density (g/cm^3)
[10] LTCC materials

Appendix B

Appendix B: ESL materials

B.1 Data-sheet of selected ESL materials for LTCC technology

Table B.1: List of used materials for LTCC technology

Material	Type
ESL41110	Low relative permittivity substrate
ESL41060	High relative permittivity substrate
ESL802	Via fill Gold conductor
ESL803	pattern Gold conductor
5873-G	Gold-Palladium conductor
ESl49000	Cavity fill fugitive material

ESL ELECTROSCIENCE
CERAMIC TAPES &
THICK-FILM MATERIALS
416 EAST CHURCH ROAD
KING OF PRUSSIA, PA 19406-2625 USA
T: 610.272.8000
F: 610.272.6759
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CO-FIRE CERAMIC TAPE 41110

RoHS Compliant Ceramic Tape for Multilayer and Microwave Applications Requiring Low Dielectric Constant

A flexible cast film of inorganic dielectric powder dispersed in an organic matrix, designed to be fired at 850°C to give a dense body. Multilayer parts can be formed by laminating metallized sheets of the tape into a monolithic structure prior to firing. A pressure/temperature combination of 21 MPa and 70°C works well for laminating this tape. Ceramic tape is provided on a silicone-coated polyester film to minimize environmental contamination, to protect it from mechanical damage, and to aid in handling. This material is useful in microwave applications that require low dielectric constant and low loss.

PROCESSING PARAMETERS

LAMINATING:	21 MPa at 70°C
FIRING TEMPERATURE:	850°C
TIME AT PEAK TEMPERATURE:	10 minutes

TAPE CHARACTERISTICS

TAPE THICKNESS:	100-130 µm
COLOR:	blue
SHELF LIFE: (when stored in dry N_2)	6 months

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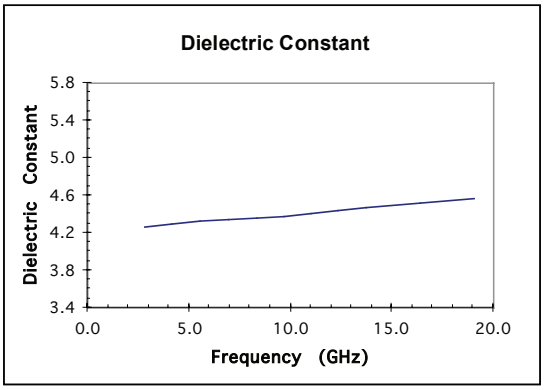
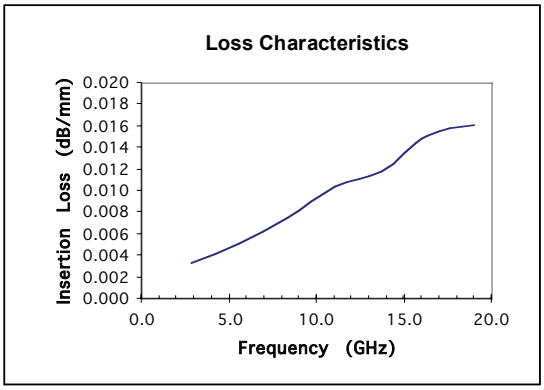
FIRED TAPE PROPERTIES (Tested with ESL 803 post-fired gold conductor)

DIELECTRIC CONSTANT: (1 MHz, using post-fired ESL 903-A silver conductor)		4.0-5.0
DIELECTRIC CONSTANT: (GHz, cofired with ESL 903-A silver conductor, see microwave properties below)		4.3-4.7
DISSIPATION FACTOR: (1 MHz, using post-fired ESL 903-A silver conductor)		≤ 0.4%
INSULATION RESISTANCE: (100 VDC)		≥ 10^{12} Ω
THERMAL CONDUCTIVITY:		2.5-3.0 W/(m·K)
TCE: (25°C to 300°C)		6.4 ppm/°C
BREAKDOWN VOLTAGE:		> 1500 V/25 µm
PRESSURE COOKER: (Insulation resistance after 15 minutes at 2 atmospheres)		≥ 10^{12} Ω
FIRED SHRINKAGE: (Using recommended processing parameters)	X and Y Z	15 ± 1% 16 ± 2%
FIRED DENSITY: (Theoretical)		2.30 g/cm^3
COMPATIBLE CONDUCTORS:		ESL 803, 902, 903-A, 903-B, 903-C, 963

MICROWAVE PROPERTIES *





* Data obtained from measurements on ring resonators. Metallization is co-fired 903-A silver.

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CO-FIRE CERAMIC TAPE 41060

Lead-Free Ceramic Fire Tape for Multilayer and Microwave Applications Requiring Dielectric Constant of 16-17

The 41060 is a flexible cast film of inorganic dielectric powder dispersed in an organic matrix, designed to be fired at 875°C to give a dense body. Multilayer parts can be formed by laminating metallized sheets of the tape into a monolithic structure prior to firing. A pressure/temperature combination of 21 MPa and 70°C works well for laminating this tape. Ceramic tape is provided on a silicone-coated polyester film to minimize environmental contamination, to protect it from mechanical damage, and to aid in handling. This dielectric is useful in microwave applications that require intermediate dielectric constant and low loss.

PROCESSING PARAMETERS

LAMINATING:	21 MPa at 70°C
FIRING TEMPERATURE:	875°C
TIME AT PEAK TEMPERATURE:	30 minutes

TAPE CHARACTERISTICS

TAPE THICKNESS:	100-130 µm
COLOR:	blue
SHELF LIFE:	6 months

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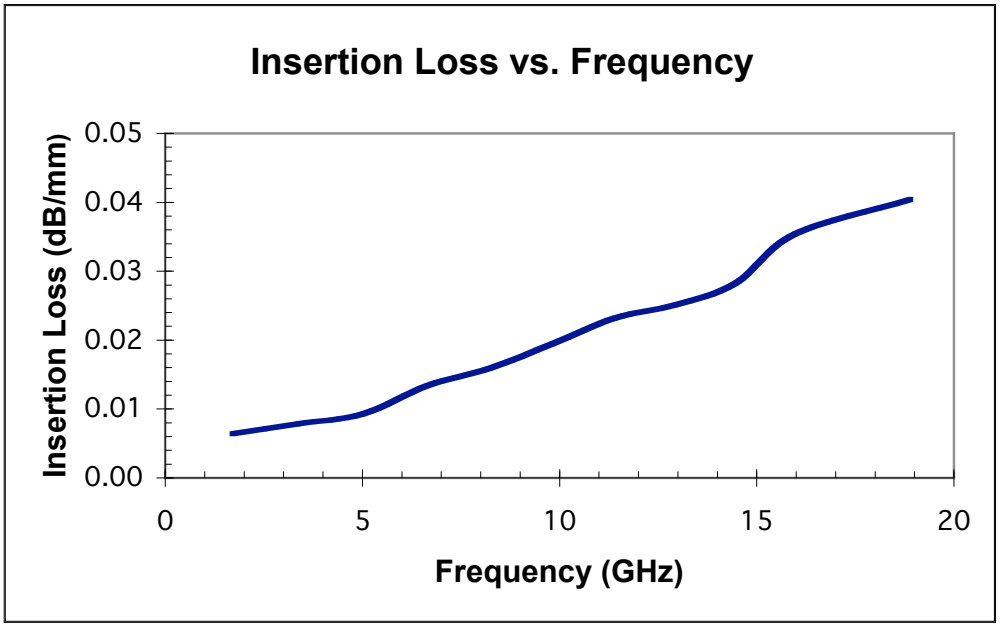
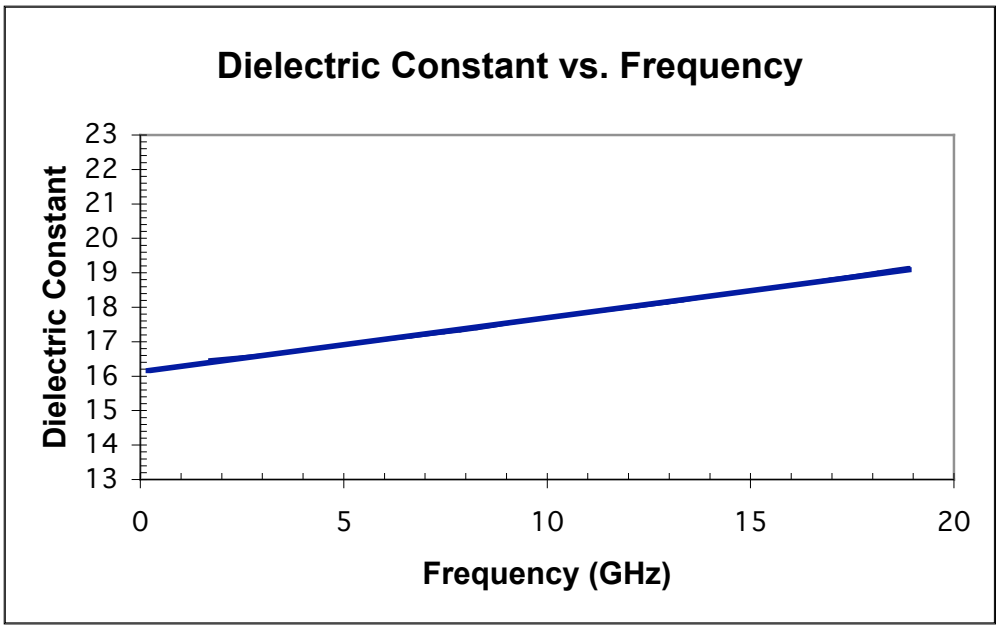
FIRED TAPE PROPERTIES (Using co-fired 903-A silver conductor)

DIELECTRIC CONSTANT: (1 MHz)		16-17
DISSIPATION FACTOR: (1 MHz)		0.2%
TCE: (25°C to 300°C)		7.55 ppm/°C
FIRED SHRINKAGE: (Using recommended processing parameters)	X and Y	9.5%±0.5%
	Z	15.0%±1.0%
FIRED DENSITY: (Theoretical)		3.46 g/cm^3
COMPATIBLE CONDUCTORS:		903-A

MICROWAVE PROPERTIES





* - Data obtained from measurements on ring resonators. Metallization is co- fired 903-A silver.

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GOLD CONDUCTORS

802-CT, 802-CTHV, 803-CT-M

Conductors for Low Temperature, Co-Fired, Ceramic Tapes

ESL 802-CT, 802-CTHV, and 803-CTM are gold conductor pastes specially developed for use with ESL Lo-Fire ceramic tapes. These materials are designed for the following requirements:

802-CT	For via fill metallization
802-CTHV	A high solids, high viscosity, via fill metallization
803-CT-M	For buried and top layer metallization

PASTE DATA

RHEOLOGY:		Thixotropic, screen printable pastes
VISCOSITY:		
(Brookfield RVT, ABZ spindle, 10 rpm, 25.5°C±0.5°C)	**802-CT**	250±50 Pa•s
(Brookfield HBT, #7 spindle, 1 rpm, 25.5°C±0.5°C)	**802-CTHV**	3500±1000 Pa•s
(Brookfield RVT, ABZ spindle, 10 rpm, 25.5°C±0.5°C)	**803-CT-M**	250±50 Pa•s
SOLIDS CONTENT:		
	802-CT	87.0%±1%
	802-CTHV	90.0%±1%
	803-CT-M	78.0%±1%
SHELF LIFE:		6 months

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PROCESSING

SCREEN MESH/EMULSION:	325/12.5 μm
LEVELING TIME: (at 25°C)	5-10 minutes
DRYING: (at 125°C)	10-15 minutes
FIRING TEMPERATURE:	Conductors are co-fired with the LTCC
SUBSTRATE FOR CALIBRATION:	LTCC
THINNER:	ESL 401

TYPICAL PROPERTIES

	802-CT	802-CTHV	803-CT-M
THICKNESS: (μm)	16-22	40-45	9-12
RESISTIVITY: (mΩ/sq.)	≤ 20	≤ 13	≤ 5
SOLDERABILITY: (Using 80 Au/20 Sn solder)	NA	NA	good
WIREBONDABILITY: (Pull strength using 25 μm Au wire)	NA	NA	≥ 10 g
ADHESION: (2 mm x 2 mm pads, pull test)	NA	NA	13.7 N

NOTES: All data was collected using ESL 41010-70C or similar tape, co-fired at 850°C.

COMPATIBILITY:

Tape	802-CT	802-CTHV	803-CT-M
41110-70C	via fill	via fill	top/inner
41020-70C	via fill	n/a	top/inner
41210-70C	n/a	n/a	top/inner

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GOLD CONDUCTOR 803

Conductor for Low Temperature Co-fired Ceramic Tapes

ESL 803 is a gold conductor paste specially developed for use with ESL low temperature co-fired ceramic tapes (LTCC). This material is designed for use as an inner layer or top layer metallization.

PASTE DATA

RHEOLOGY:	Thixotropic, screen-printable paste
VISCOSITY: (Brookfield RVT, ABZ spindle, 10 rpm, 25.5 ± 0.5 °C)	225 ± 50 Pa.s
SOLIDS CONTENT:	77.0 ± 1.5 %
SHELF LIFE: (at 25 °C)	6 months

PROCESSING

SCREEN MESH/EMULSION:	325 / 25 ± 12 µm
LEVELING TIME: (at 25°C)	5 - 10 min
DRYING TIME: (at 80°C)	10 -15 min
FIRING TEMPERATURE:	Co-fired with LTCC
RATE OF ASCENT/DESCENT:	60°C - 100°C/minute
SUBSTRATE FOR CALIBRATION:	ESL 41010
THINNER:	ESL 401

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TYPICAL PROPERTIES

FIRED THICKNESS: (measured on a 2 mm x 2 mm pad)	6 - 12 µm
RESISTIVITY: (measured on a 100 mm x 0.25 mm conductor track at 9 µm fired thickness)	≤ 10 mΩ/square
SOLDER WETTABILITY: (80 Au / 20 Sn solder)	Good
WIREBONDABILITY: (25 µm Au wire) **INITIAL PULL STRENGTH:**	≥ 10 grams
ADHESION: (90º pull, 2.0 mm x 2.0 mm pads) **INITIAL PULL STRENGTH:**	≥ 13 N

NOTES: All data was collected using ESL 41010 or similar tape, co-fired at 850ºC.

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CERMET PLATINUM / GOLD CONDUCTOR 5837-G

Cadmium, Lead & Nickel-Free*

ESL 5837-G is a platinum gold conductor that is solderable both on 96% alumina substrates and when fired over 4917 dielectric. The 5837-G can be used in high reliability multilayer circuits where chip carriers are soldered to the top layer. The re-fire capability on alumina is also high. A typical lead and cadmium-free system consists of 8844-G gold conductor, 4917 dielectric and 5837-G. The 5837-G can also be used on beryllia substrates with excellent initial adhesion. However, the aged adhesion is lower than that obtained on 96% alumina substrates. This may be improved by firing at 980°C.

PASTE DATA

Rheology:	Thixotropic, screen-printable paste
Viscosity: (Brookfield RVT, 10rpm, ABZ spindle, 25.5 ± 0.5 °C)	250 ± 25 Pa.s
Bonding Mechanism:	Mixed-bonded
Shelf Life (20 - 25 °C):	6 months

PROCESSING

Screen Mesh, Emulsion:		325 S/S, 20 µm
Levelling Time (at 20°C):		5 - 10 min
Drying Time (at 125°C):		10 -15 min
Firing Temperature Range:		850 - 1000°C in air
	Optimum:	850°C
	Time at peak:	10 min
Total Firing Cycle:		1 hour
Substrate for Calibration:		96% alumina
Thinner:		ESL 401

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TYPICAL PROPERTIES

Fired Thickness: (measured on a 2 mm x 2 mm pad on 96% alumina)		12.0 ± 2.0 µm
Approximate Coverage:		55 - 70 cm^2/g
Resistivity:		<85 mΩ/□
Printing Resolution: (line / space)		0.125 mm / 0.125 mm
Solder Wettability: (RMA flux, 5 sec. dip, 95.5Sn/3.8Ag/0.7Cu, 250°C)	96% alumina	95 - 100 %
	over 4917	90 - 95 %
Solder Leach: (No. of 10 sec. dips to double minimum resistance of 100 mm x 0.25 mm conductor, 95.5Sn/3.8Ag/0.7Cu, 250°C)		> 6 dips

Adhesion:
(90° pull, 2 mm x 2 mm pads, 95.5Sn/3.8Ag/0.7Cu)

Initial pull strength:	on 96% alumina	>7.0 kg
Aged 48 hours at 150°C:	on 96% alumina	>4.0 kg
Initial pull strength:	on 4917	>4.0 kg
Aged 48 hours at 150°C:	on 4917	>3.0 kg

***Complies with RoHS, ELV, WEEE and CHIP 3 EC directives.**

CAUTION: Proper industrial safety precautions should be exercised in using these products. Use with adequate ventilation. Avoid prolonged contact with skin or inhalation of any vapours emitted during use or heating of these compositions. The use of safety eye goggles, gloves or hand protection creams is recommended. Wash hands or skin thoroughly with soap and water after using these products. Do not eat or smoke in areas where these materials are used. Refer to appropriate MSDS sheet.

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FUGITIVE TAPE 49000

Organic-Based Tape for use in Creating Channels in Sensors

ESL 49000 is a flexible cast film of fugitive powder dispersed in an organic matrix. This material is designed to be burned out in the temperature range of 600°C-700°C to yield a void where the tape was placed. ESL 49000 tape is provided on a silicone-coated polyester film to protect the tape from mechanical damage and aid in handling.

This tape is generally used with zirconia or alumina green tapes and can be co-fired for use in oxygen sensors.

TAPE THICKNESS: 125µm +/- 10%
(custom thicknesses available)

PROCESSING:

Parts are formed by blanking sheets of the tape to the required green size prior to firing. The burnout cycle depends on the part configuration and size.

TYPICAL FIRING PROFILE FOR PARTS: Depends on matrix tapes

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Appendix C

Appendix C: LC matching network calculation

The LC-section matching network is used for large frequency bands and depend on the load impedance (z_L) relative to normalized impedance (Z_0). As represented in the Figure C.1, two configurations are available for network elements calculation:

- $RL < Z_0 \Rightarrow$ Load impedance is outside the $r = 1$ circle on the SMITH chart
- $RL > Z_0 \Rightarrow$ Load impedance is inside the $r = 1$ circle on the SMITH chart

In the first case ($RL < Z_0$), two solution are obtained and the network elements are calculated according to the input impedance Z_{in}

$$Z_{in} = Z_0 = jX + \frac{1}{jB + \frac{1}{R_L + jX_L}} \tag{C.1}$$

$$B = \frac{X_L \pm \sqrt{R_L/Z_0}\sqrt{R_L^2 + X_L^2 - Z_0 R_L}}{R_L^2 + X_L^2} \tag{C.2}$$

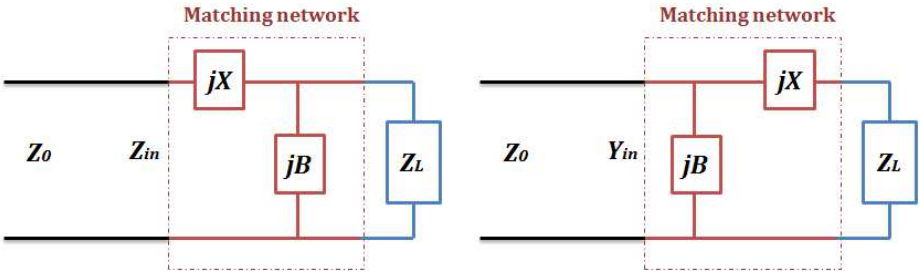
$$X = \frac{BZ_0R_L - X_L}{1 - BX_L} \tag{C.3}$$

In the second case ($RL > Z_0$), two solution are also obtained and the network elements are calculated according to the input admittance Y_{in}

$$Y_{in} = \frac{1}{Z_0} = jB + \frac{1}{R_L + j(X + jX_L)} \tag{C.4}$$

$$B = \pm \frac{1}{Z_0} \sqrt{\frac{(Z_0 - R_L)}{R_L}} \tag{C.5}$$

$$X = \pm \sqrt{R_L(Z_0 - R_L)} - X_L \tag{C.6}$$



(a) (b)

Figure C.1: L matching network calculation: (a) z_L inside the $1 + jx$ circle. (b) z_L outside the $1 + jx$ circle